

Schematics Page Index (Title / Revision / Change Date)

Page	Title of Schematics Page	Rev.	Date	Page	Title of Schematics Page	Rev.	Date
1	Schematics Page Index	1.00	2006/04/10	41	ICH7-M(GND) 5/5	1.00	2006/04/10
2	Block Diagram	1.00	2006/04/10	42	SATA HDD RAID	1.00	2006/04/10
3	CLOCK GEN	1.00	2006/04/10	43	PATA CD-ROM	1.00	2006/04/10
4	Yonah(HOST BUS) 1/2	1.00	2006/04/10	44	PCI (PCI BUS)	1.00	2006/04/10
5	Yonah(HOST BUS) 2/3	1.00	2006/04/10	45	PCI (ILINK)	1.00	2006/04/10
6	Yonah(Power/Gnd) 3/3	1.00	2006/04/10	46	PCI (MS-STD/DUO/MDC/SD)	1.00	2006/04/10
7	CALISTOGA (HOST) 1/7	1.00	2006/04/10	47	PCI (PCMCIA)	1.00	2006/04/10
8	CALISTOG (DMI) 2/7	1.00	2006/04/10	48	Bluetooth	1.00	2006/04/10
9	CALIST (GRAPHIC) 3/7	1.00	2006/04/10	49	Mini-PCIE Card	1.00	2006/04/10
10	CALISTOGA (DDR2) 4/7	1.00	2006/04/10	50	EXPRESS/CAM/UIDE	1.00	2006/04/10
11	CALIST (POWER,VCC) 5/7	1.00	2006/04/10	51	LAN (82562GT)	1.00	2006/04/10
12	CALIST (VCC CORE) 6/7	1.00	2006/04/10	52	USB2.0	1.00	2006/04/10
13	CALIST (VSS) 7/7	1.00	2006/04/10	53	USB HUB 1.1	1.00	2006/04/10
14	DDR2(SO-DIMM 0) 1/3	1.00	2006/04/10	54	CIR Reciver	1.00	2006/04/10
15	DDR2(SO-DIMM 1) 2/3	1.00	2006/04/10	55	AUDIO(CODEC & POWER)	1.00	2006/04/10
16	DDR2(Termination) 3/3	1.00	2006/04/10	56	AUDIO(AMP & HP & SPK)	1.00	2006/04/10
17	VGA(PCI-E)	1.00	2006/04/10	57	AUDIO (MUTE & INTMIC)	1.00	2006/04/10
18	VGA(STRAP)	1.00	2006/04/10	58	AUDIO (PHONE OUT)	1.00	2006/04/10
19	VGA(GDDR)	1.00	2006/04/10	59	Audio BOARD conn	1.00	2006/04/10
20	VGA(MULTIUSE)	1.00	2006/04/10	60	EC+KBC	1.00	2006/04/10
21	VGA(LVD/VDAC)	1.00	2006/04/10	61	Flash ROM/XBUS	1.00	2006/04/10
22	VRAM(GDDR) # 1/2	1.00	2006/04/10	62	FAN	1.00	2006/04/10
23	VRAM(GDDR) # 2/2	1.00	2006/04/10	63	Daughter Board Conn.	1.00	2006/04/10
24	VGA(POWER) 1/3	1.00	2006/04/10	64	DOCKING CONN.	1.00	2006/04/10
25	VGA(POWER) 2/3	1.00	2006/04/10	65	Power Design Diagram	1.00	2006/04/10
26	VGA(POWER) 3/3	1.00	2006/04/10	66	DCIN&Charger	1.00	2006/04/10
27	VRAM(BYPASS) 1/2	1.00	2006/04/10	67	SYS Power (+3 3V/+5V)	1.00	2006/04/10
28	VRAM(BYPASS) 2/2	1.00	2006/04/10	68	SYS Power(+1 5V/+1 05V)	1.00	2006/04/10
29	TVIN and OUT/Semi-PnP	1.00	2006/04/10	69	DDR2 Power(+1 8V/+0 3V)	1.00	2006/04/10
30	CRT	1.00	2006/04/10	70	CPU Vcore ---MAX8771	1.00	2006/04/10
31	LVDS	1.00	2006/04/10	71	Others power plan	1.00	2006/04/10
32	MINI PCI (TV)	1.00	2006/04/10	72	OVF protection	1.00	2006/04/10
33	Hot plug behavior & IDC ARRANGEMENT block diagram	1.00	2006/04/10	73	VGA POWER(+1 1V/ +1 2V)	1.00	2006/04/10
34	HDMI Silicon 1930	1.00	2006/04/10	74	HOLE & BOSS	1.00	2006/04/10
35	HDMI Microcontroller	1.00	2006/04/10	75	HISTORY(EVT)	1.00	2006/04/10
36	HDMI UCODEC	1.00	2006/04/10	76	HISTORY(DVT)	1.00	2006/04/10
37	ICH7-M(PCI/USB) 1/5	1.00	2006/04/10	77	HISTORY(PVT)	1.00	2006/04/10
38	ICH7-M(LPC,IDE,SATA)2/5	1.00	2006/04/10	78	HISTORY(MP)	1.00	2006/04/10
39	ICH7-M(GPIO) 3/5	1.00	2006/04/10	79	Power On Sequence Block Diagram	1.00	2006/04/10
40	ICH7-M(POWER) 4/5	1.00	2006/04/10	80	Power On Sequence Timing	1.00	2006/04/10

P. Leader	Check by	Design by
紀博文	楊志川	楊志川

FOXCONN		HON HAI Precision Ind. Co., Ltd.
Index Page		CUTPG - R&D Division
Rev	Document Name	Rev
1.00	MS20-1-01 Main Board (MS20-101)	1.00
Date: 2006/04/10		

Project Code & Schematics Subject: MS20 MP Main Board

PCB P/N: 1P-0064100-8011 (FUBAI)
1P-1064506-8011 (HANSTAR)

Schematics Page Index (Title / Revision / Change Date)							
Page	Title of Schematics Page	Rev.	Date	Page	Title of Schematics Page	Rev.	Date
01	Schematics Page Index	1.00	2006/04/10	41	ICH7-M(GND) 5/5	1.00	2006/04/10
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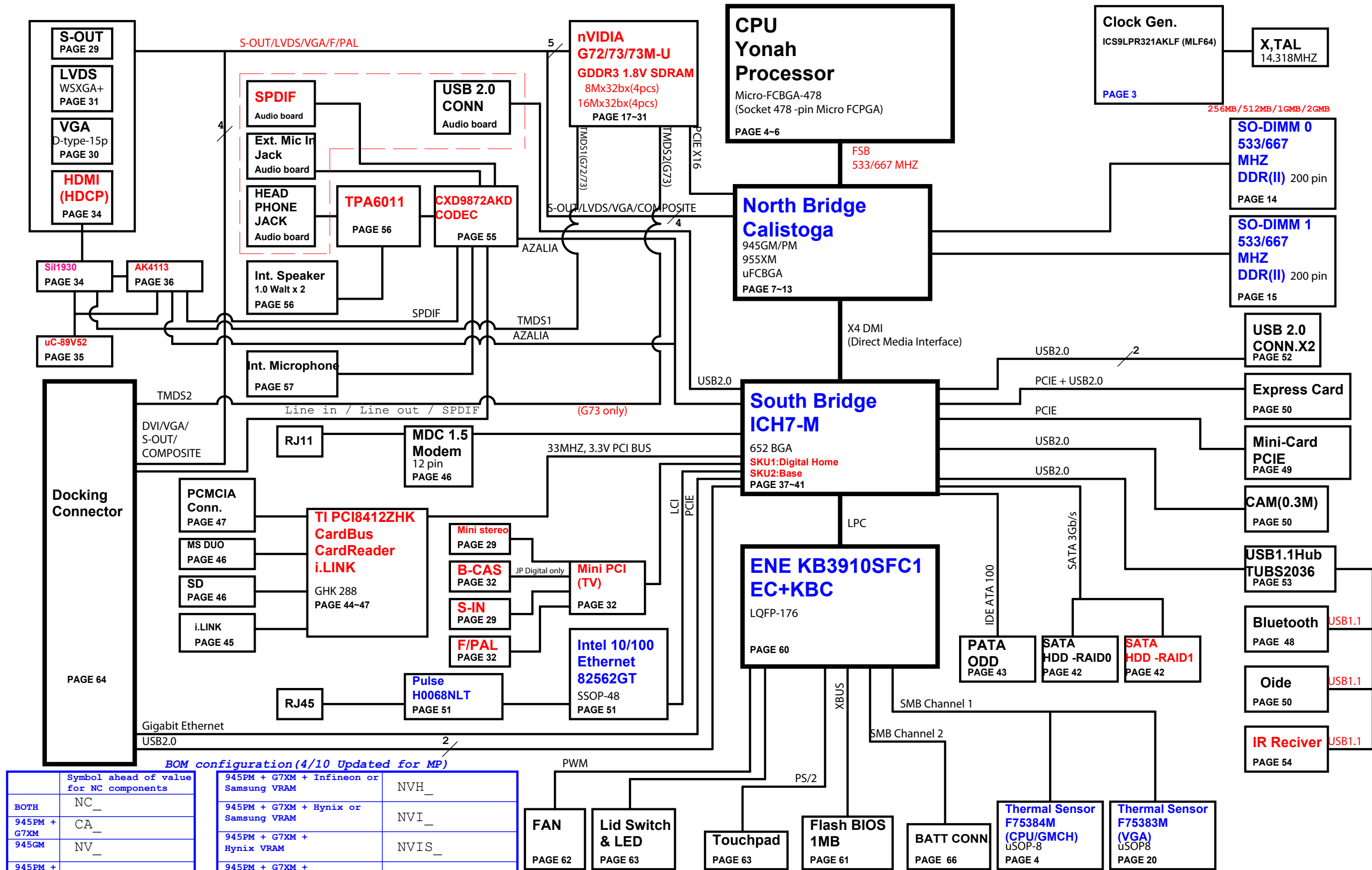
P. Leader	Check by	Design by

Project Code & Schematics Subject:	MS20 MP Main Board	PCB P/N:	1P-0064100-8011 (FUBAI) 1P-1064506-8011 (HANSTAR)
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FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title Index Page		
Size: A3	Document Number (MS20-1-01)MainBoard (MBX-156)	Rev 1.00
Date: Friday, April 14, 2006 Sheet 1 of 80		

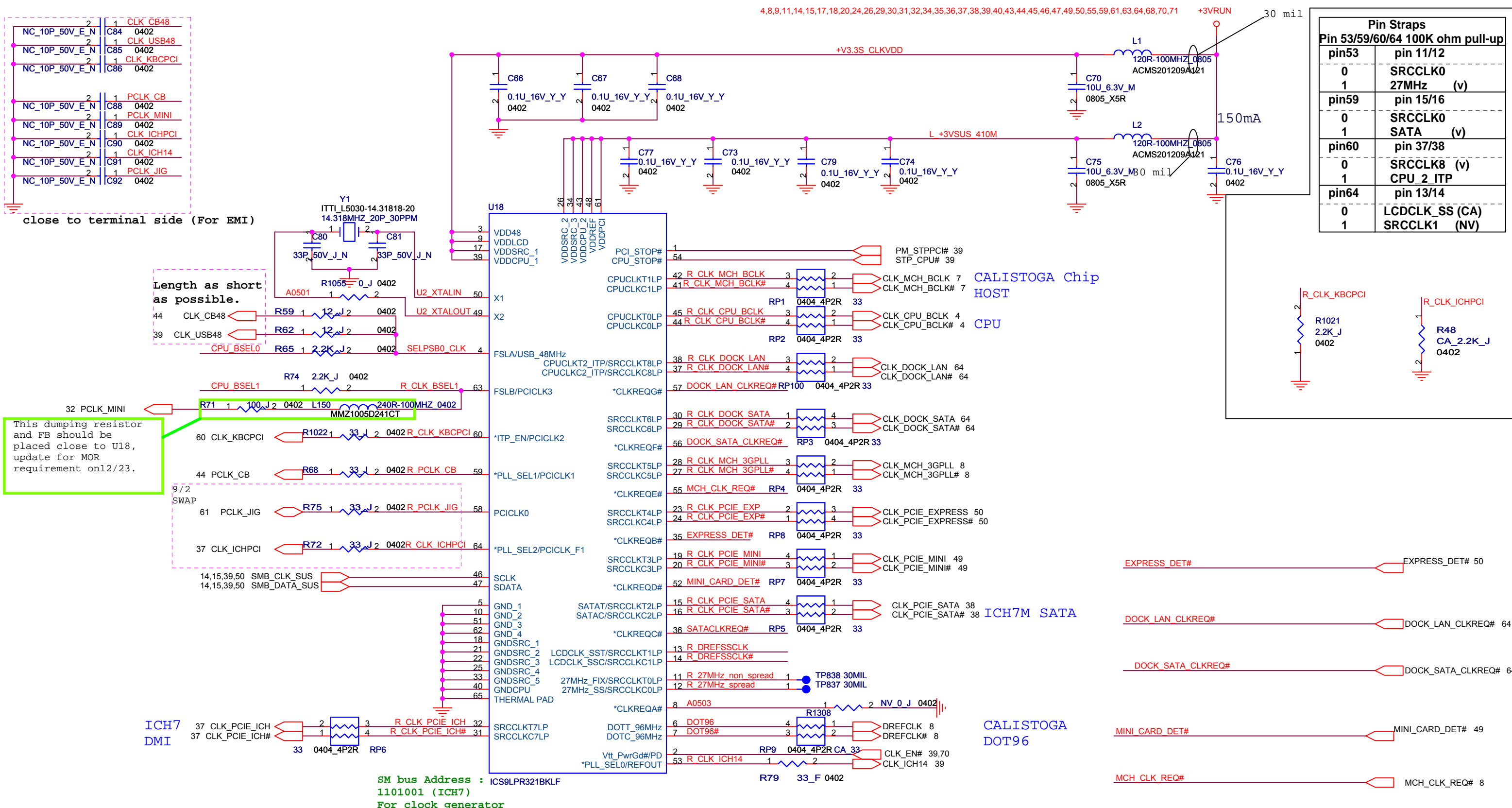
MS20(CALISTOGA PM/GM+Gfx Block Diagram)

Red texts:
New modified



BOM configuration(4/10 Updated for MP)

	Symbol ahead of value for NC components	
BOTH	NC_	945PM + G7XM + Infineon or Samsung VRAM
945PM + G7XM	CA_	945PM + G7XM + Hynix or Samsung VRAM
945GM	NV_	945PM + G7XM + Hynix VRAM
945PM + G72M	NV73_	945PM + G7XM + Infineon VRAM
945PM + G73M	NV72_	945PM + G72M or G73M
945PM + G72M or G73M-U	NV73Only_	945PM + G73M-U
		*JP Digital TV Tuner SKU & No Tuner SKU not stick
		JD TVNC_



This dumping resistor and FB should be placed close to U18, update for MOR requirement on12/23.

Length as short as possible.

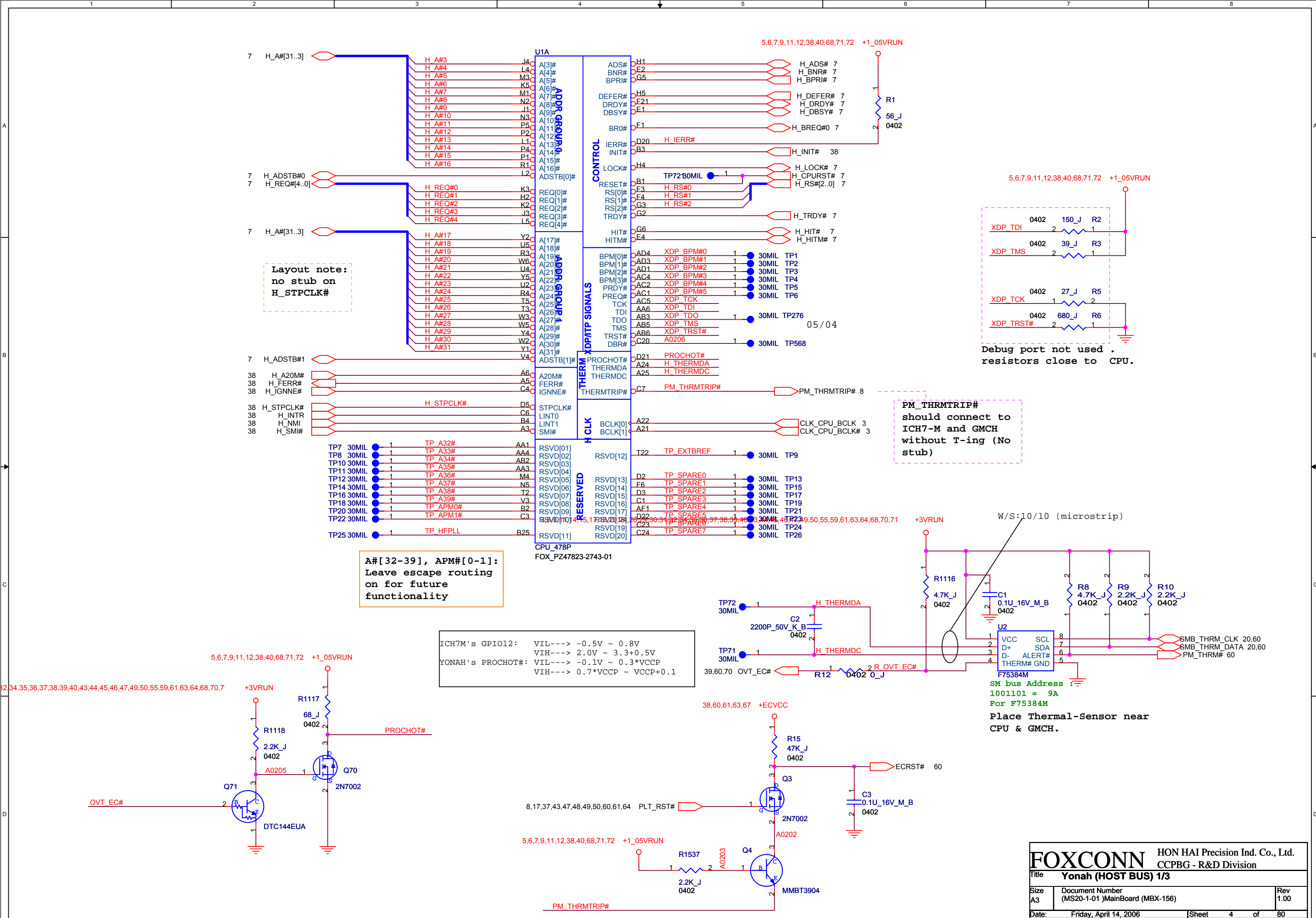
close to terminal side (For EMI)

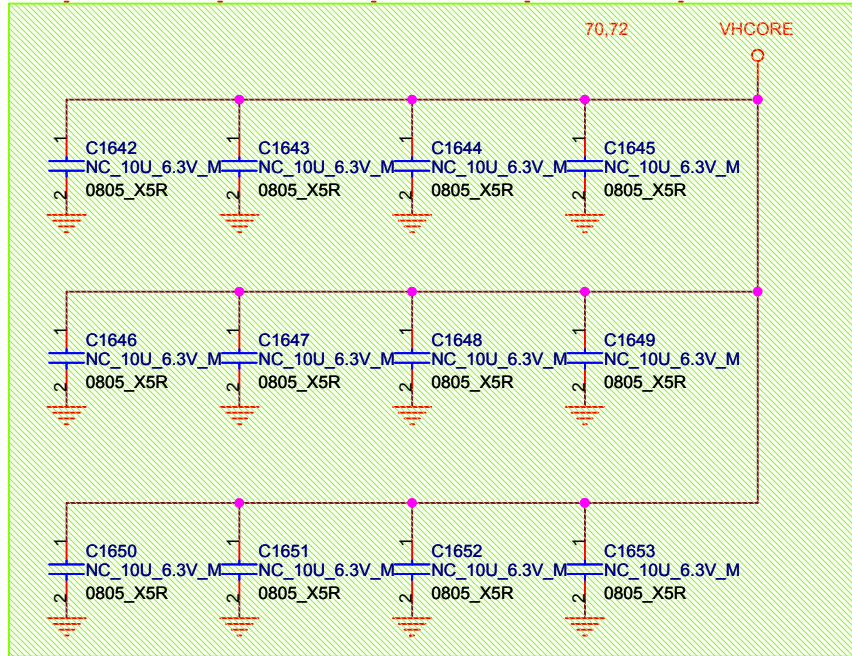
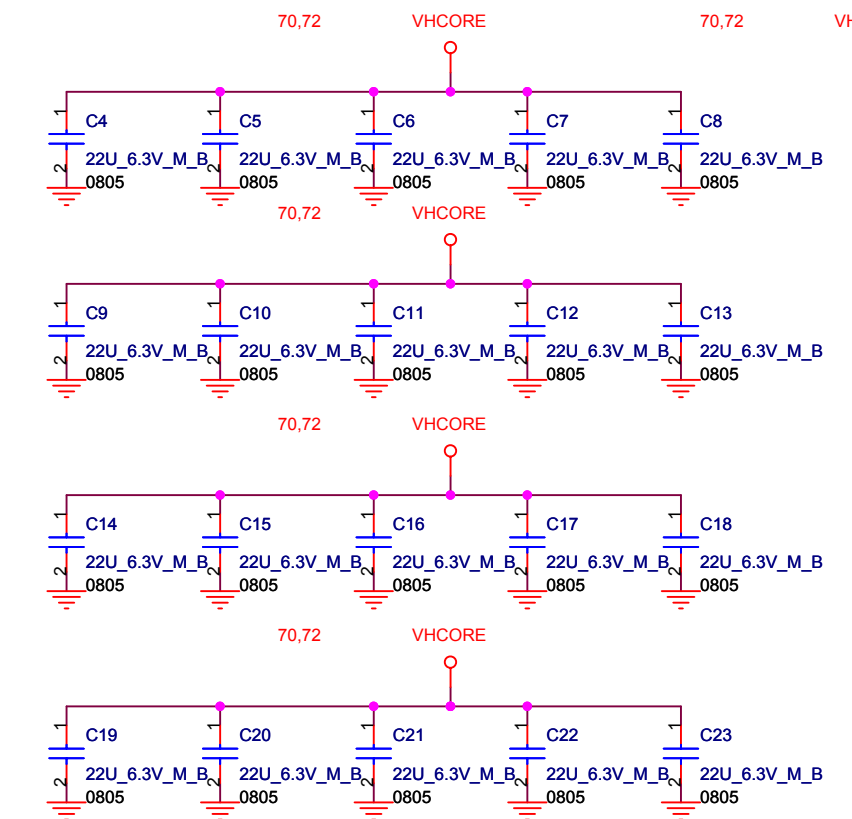
FSB Frequency Table:

FSLB	FSLA	CPU SRC[7:0]	PCI
0	0	100	100 33
0	1	133	100 33
1	0	200	100 33
1	1	166	100 33

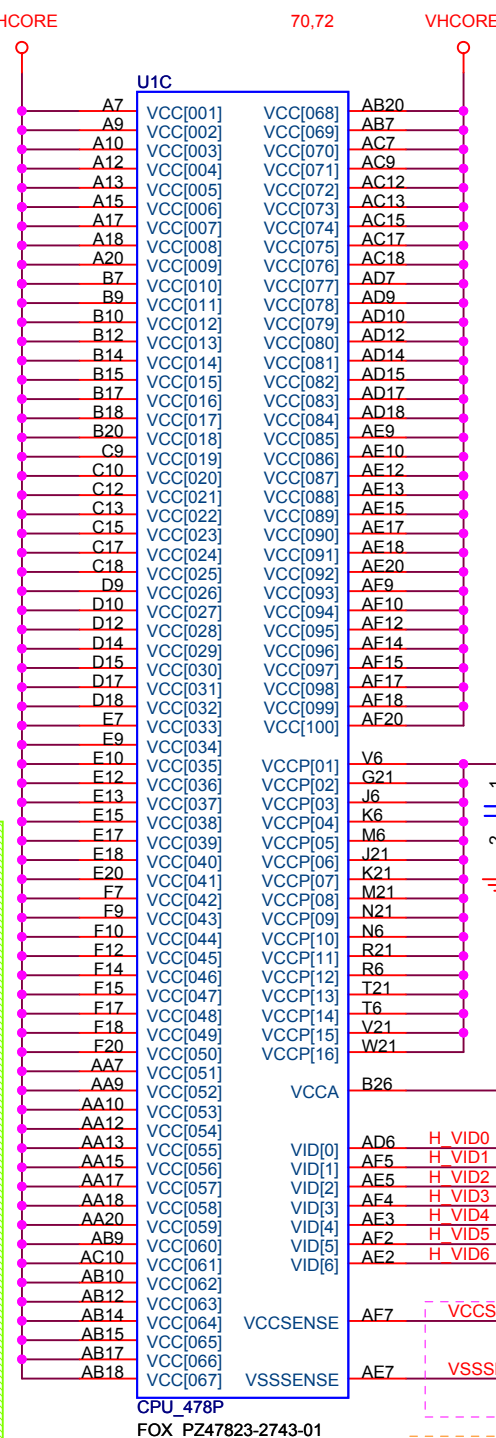
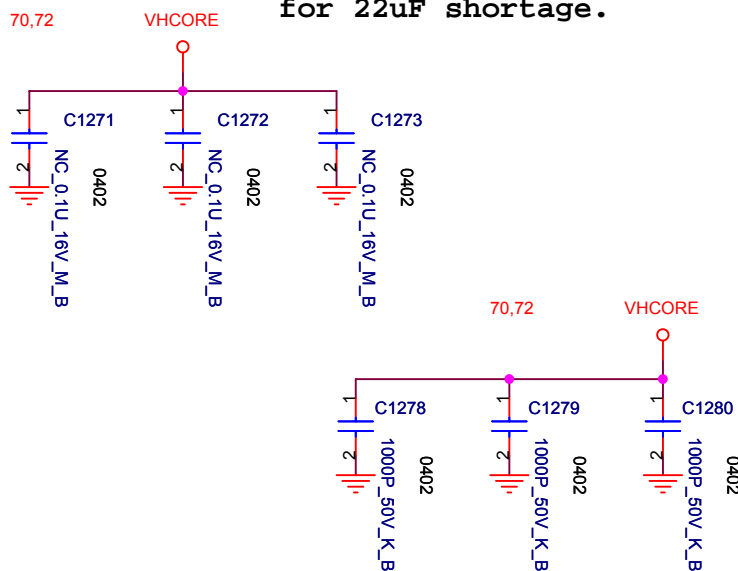
Pin Straps
Pin 53/59/60/64 100K ohm pull-up

pin53	pin 11/12
0 1	SRCCLK0 27MHz (v)
pin59	pin 15/16
0 1	SRCCLK0 SATA (v)
pin60	pin 37/38
0 1	SRCCLK8 (v) CPU_2 ITP
pin64	pin 13/14
0 1	LCDCLK_SS (CA) SRCCLK1 (NV)

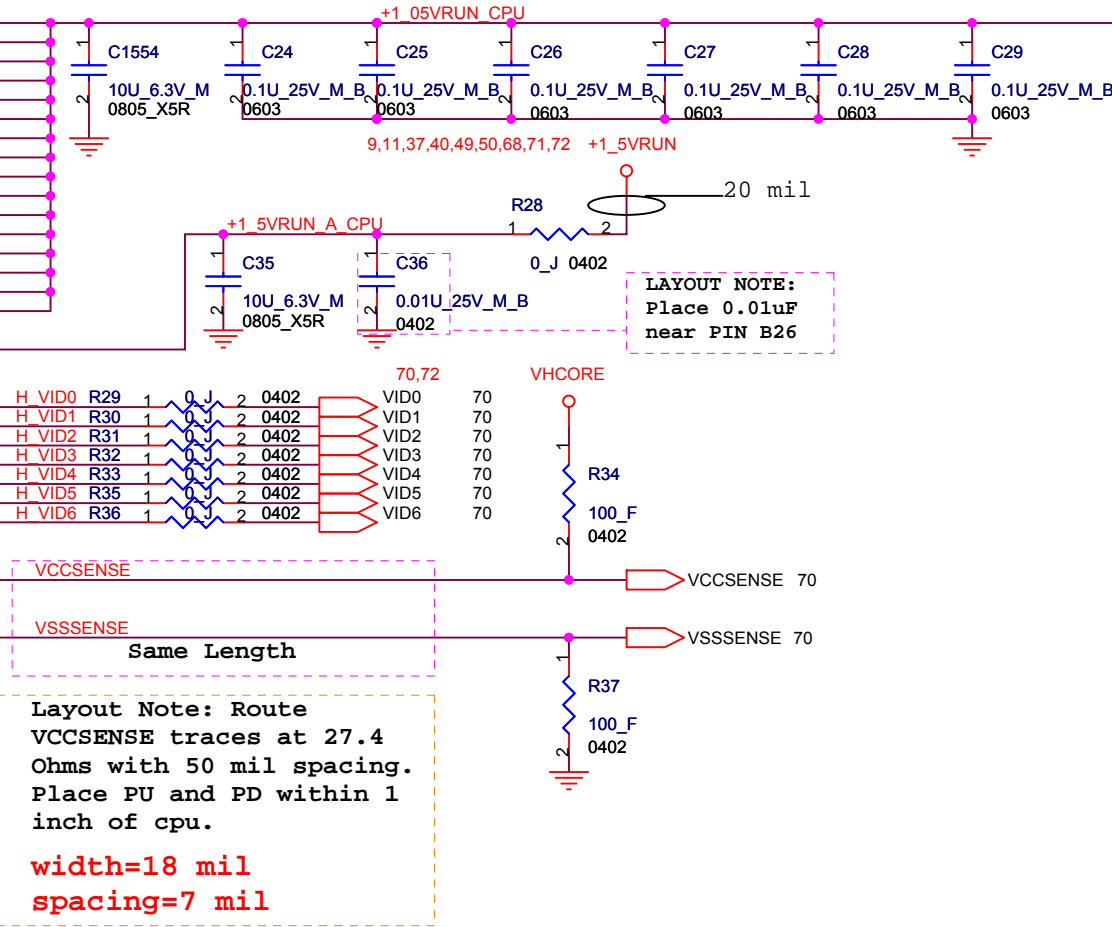




022706: Backup 10uF capacitors for 22uF shortage.



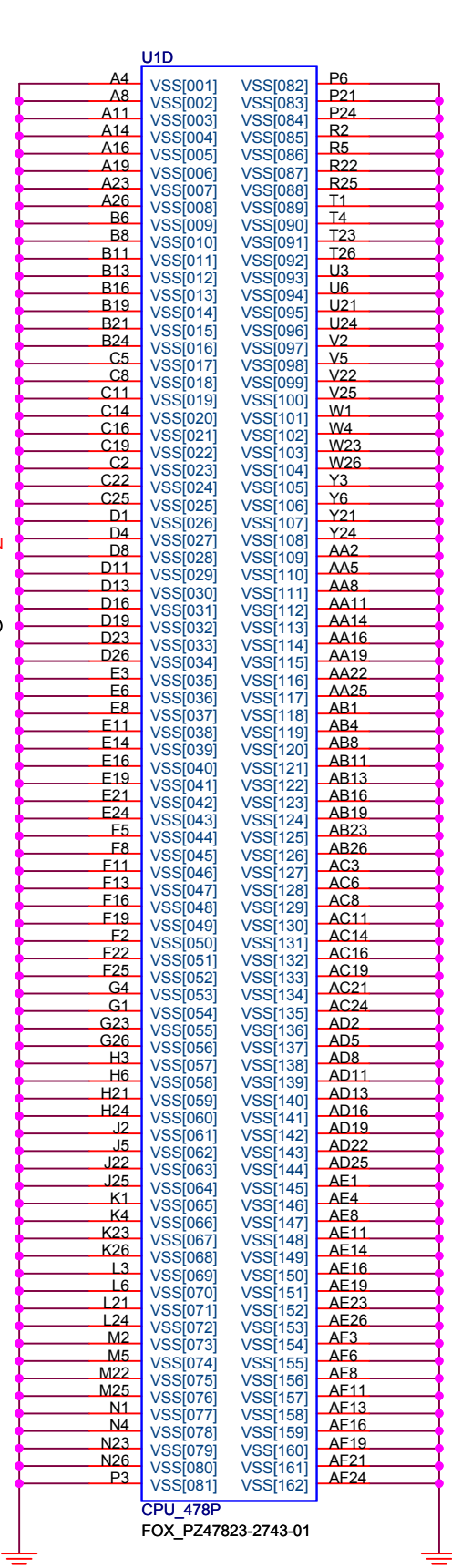
CPU_VCCA----->120mA
CPU_VCCP----->2.5A
CPU_VCC----->44A

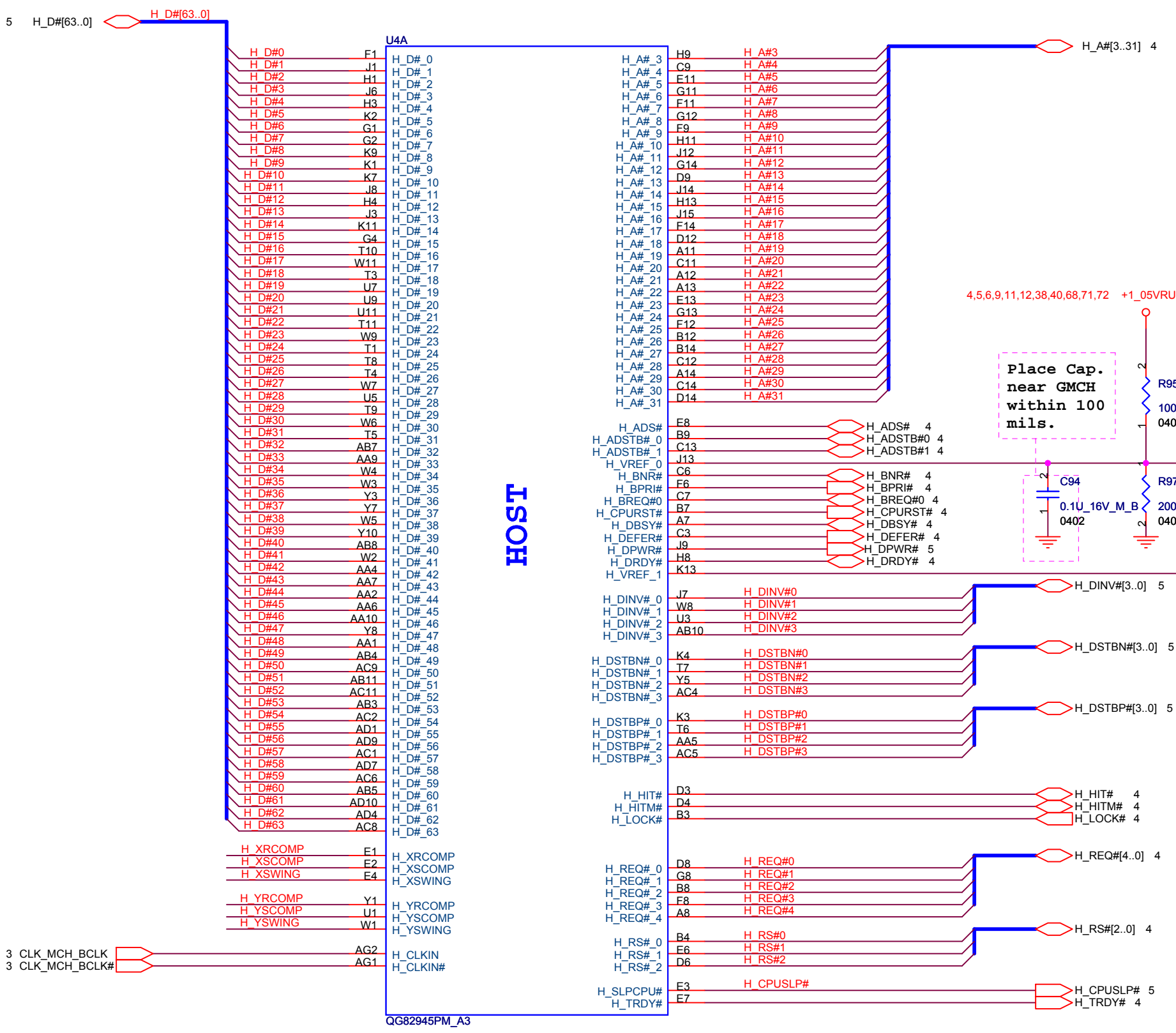


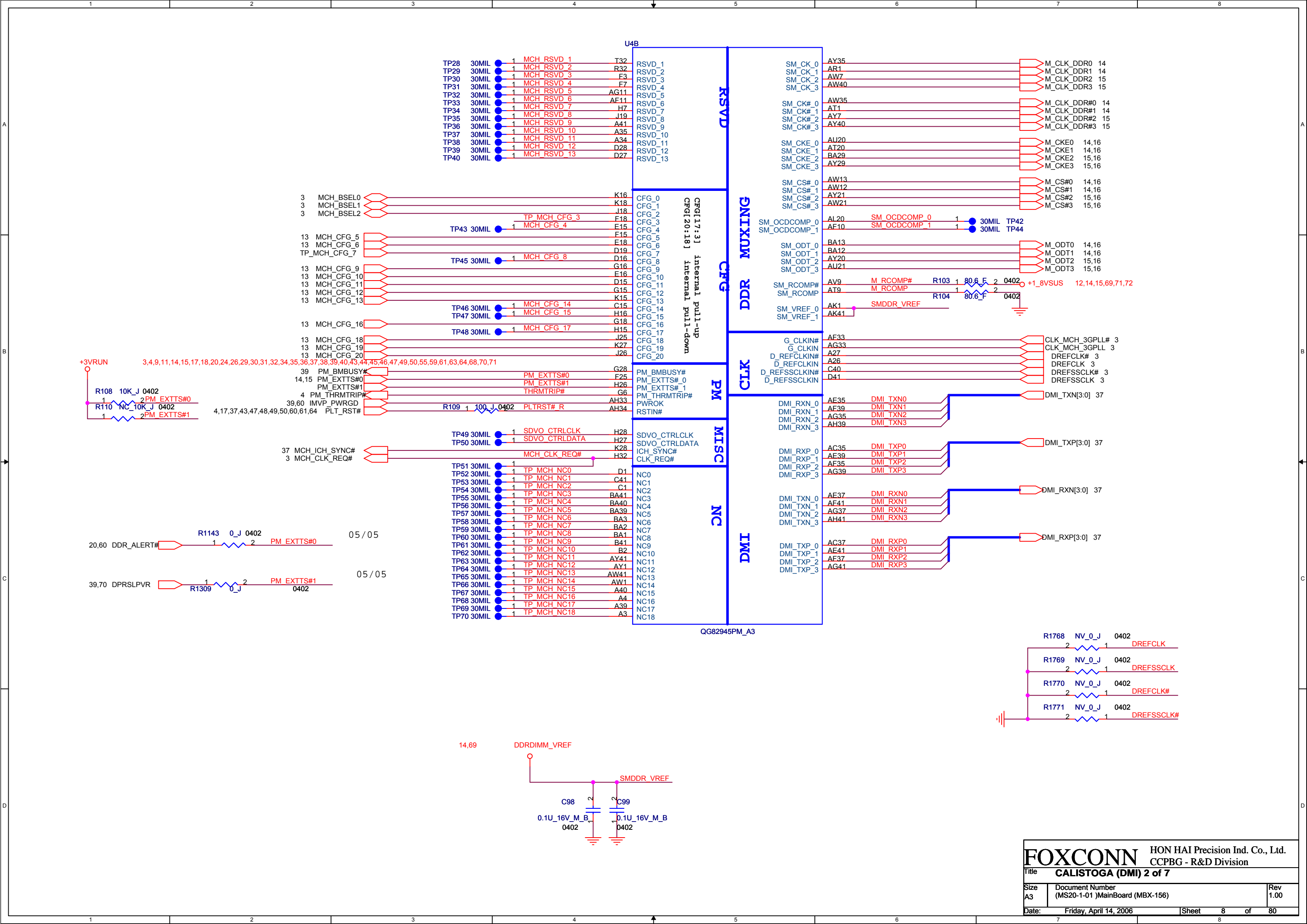
LAYOUT NOTE:
Place 0.01uF near PIN B26

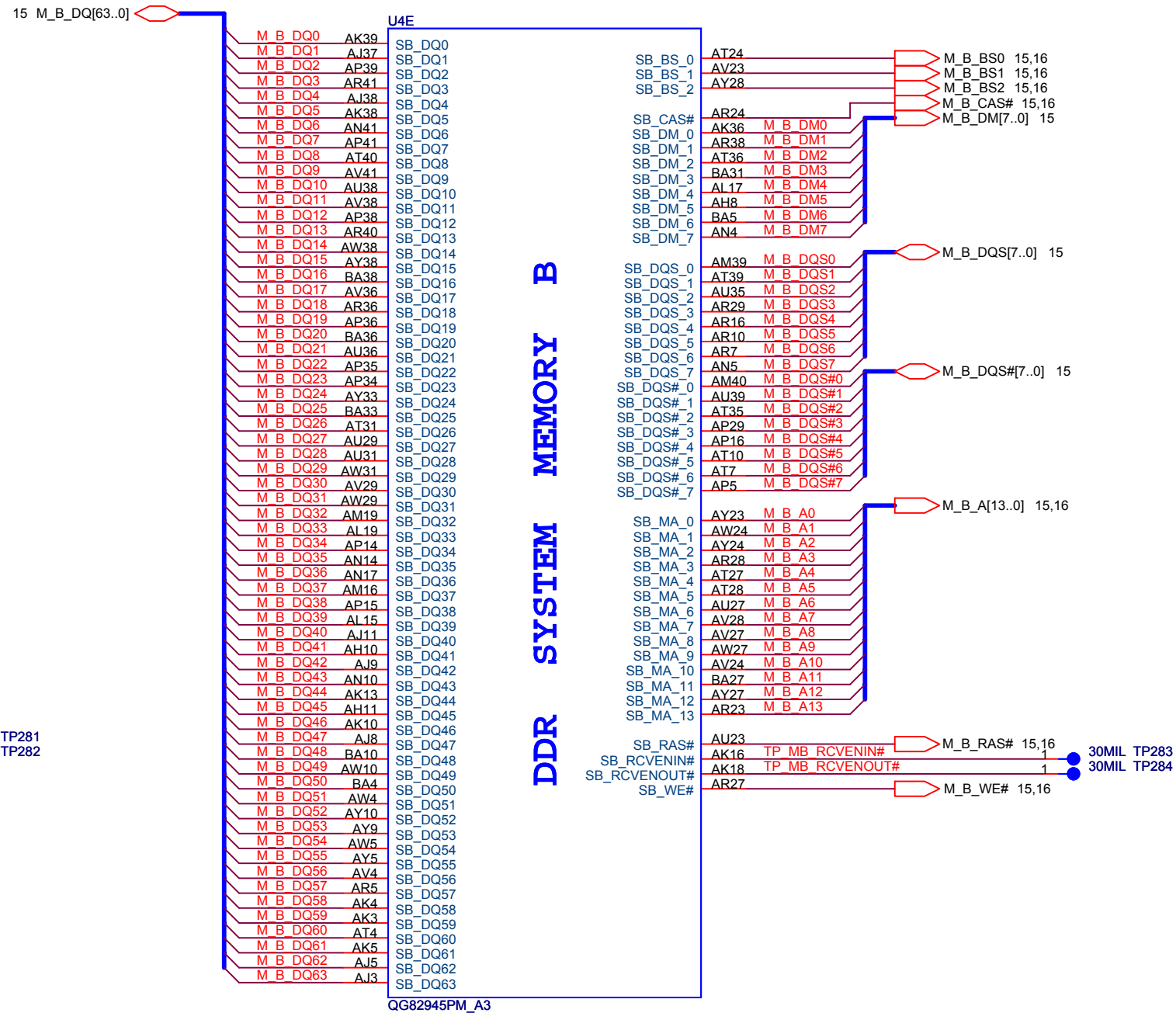
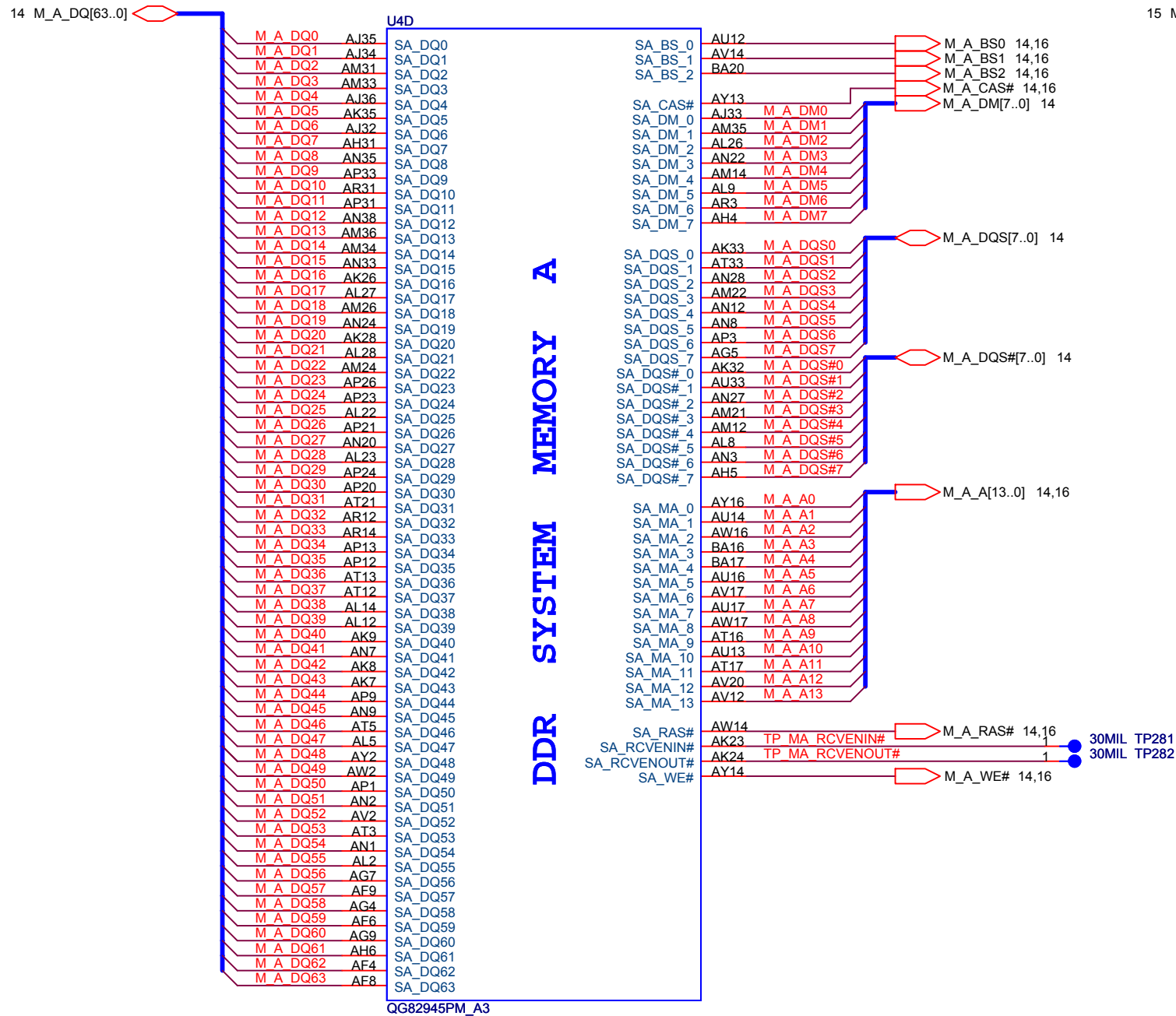
Layout Note: Route VCCSENSE traces at 27.4 Ohms with 50 mil spacing. Place PU and PD within 1 inch of cpu.
width=18 mil
spacing=7 mil

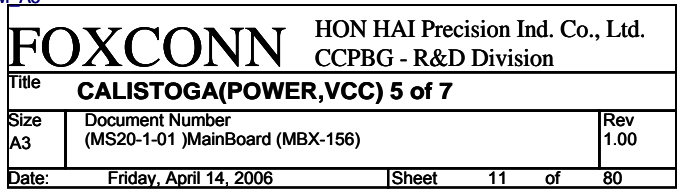
100 mil

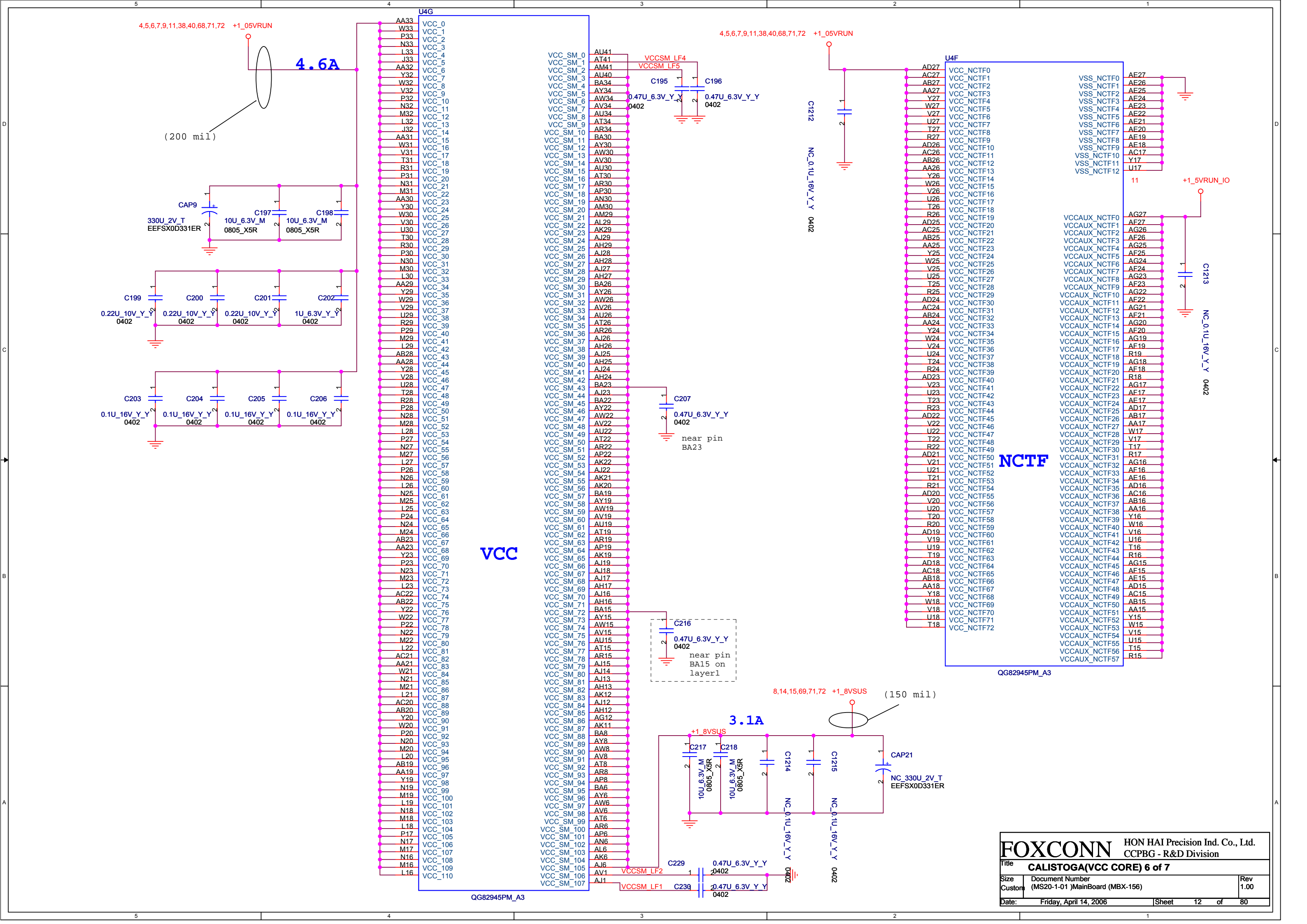












8 MCH_CFG_5 ◀ 1 30MIL TP554

MCH_CFG_5	Low = DMIx2 High = DMIx4
-----------	-----------------------------

8 MCH_CFG_6 ◀ 1 30MIL TP556

MCH_CFG_6	Low = Moby Dick High = Calistoga DDR2 select (default high)
-----------	---

8 TP_MCH_CFG_7 ◀ TP MCH CFG 7

MCH_CFG_7 (CPU Strap)	Low = RSVD High = Mobile Yonah processor
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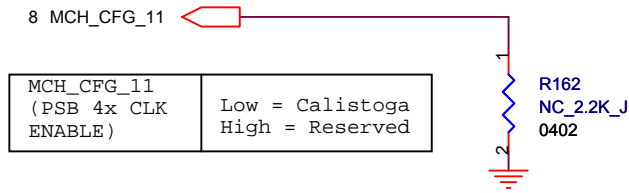
8 MCH_CFG_9 ◀ 1 30MIL TP559

MCH_CFG_9 (PCIE Graphics Lane)	Low = Reverse Lane High = Normal operation
-----------------------------------	---

For layout convenience

8 MCH_CFG_10 ◀ 1 30MIL TP560

MCH_CFG_10 (HOST PLL VCC SELECT)	Low = RESERVED High = MOBILITY
-------------------------------------	-----------------------------------



8 MCH_CFG_12 ◀ 1 30MIL TP562
8 MCH_CFG_13 ◀ 1 30MIL TP563

MCH_CFG_[13:12] (XOR/ALLZ)	00=Partial Clock Gating Disable 01=XOR Mode Enable 10=All-Z Mode Enable 11=Normal Operation(Default)
-------------------------------	---

8 MCH_CFG_16 ◀ 1 30MIL TP564

MCH_CFG_16 (FSB Dynamic ODT)	Low = Dynamic ODT Disabled High = Dynamic ODT Enable
---------------------------------	---

MCH_CFG_18 (VCC_CORE Select)	Low = 1.05V(default) High = 1.5V
---------------------------------	-------------------------------------

8 MCH_CFG_18 ◀ 1 30MIL TP555

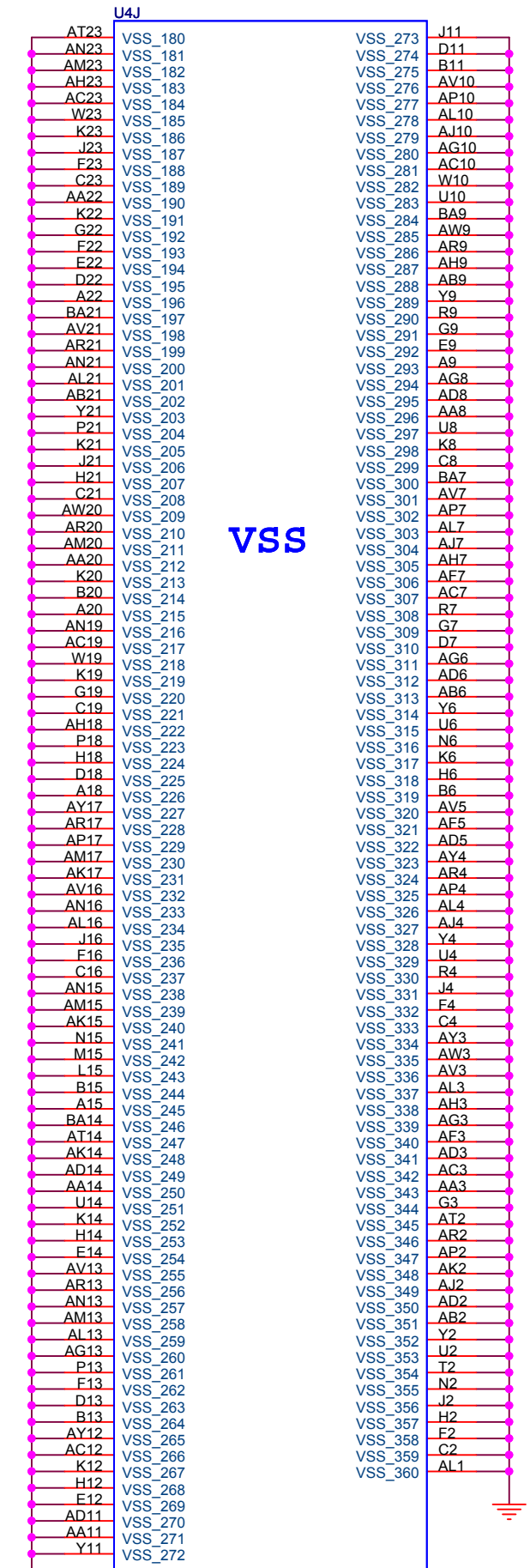
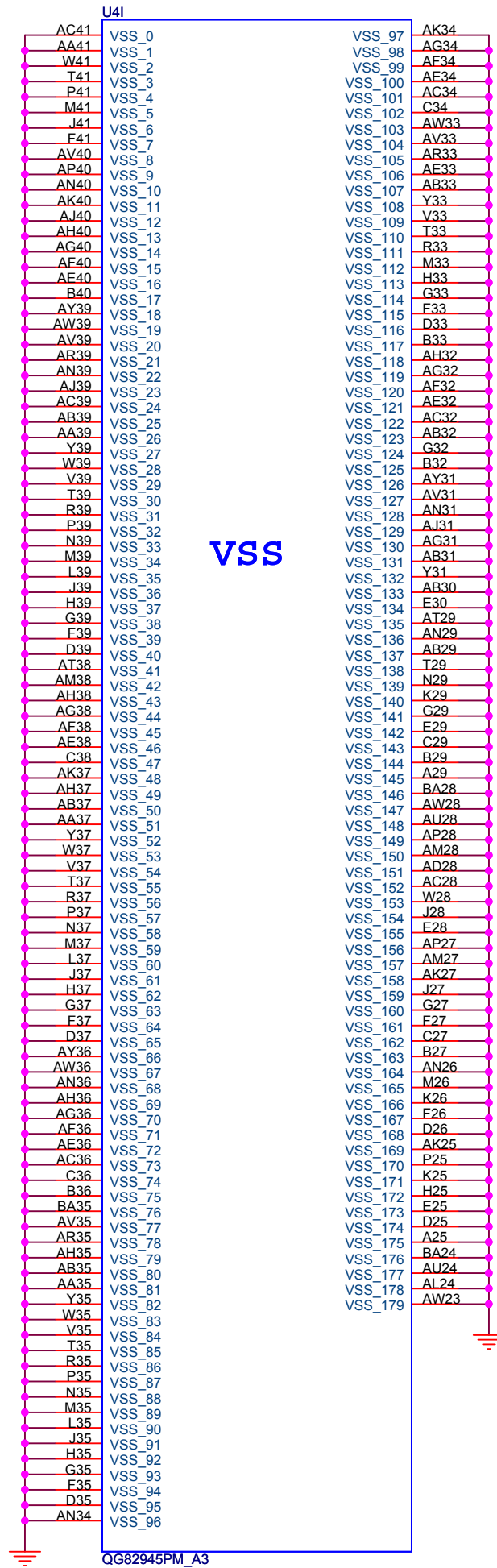
MCH_CFG_19 (DMI LANE REVERSAL)	Low = Normal(default) High = LANES REVERSED
-----------------------------------	--

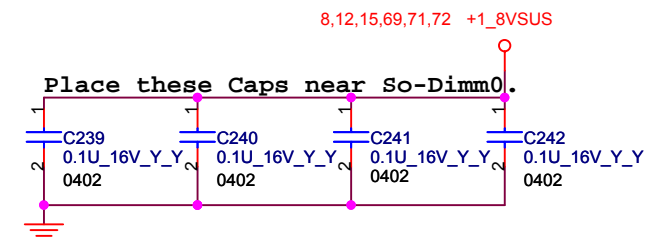
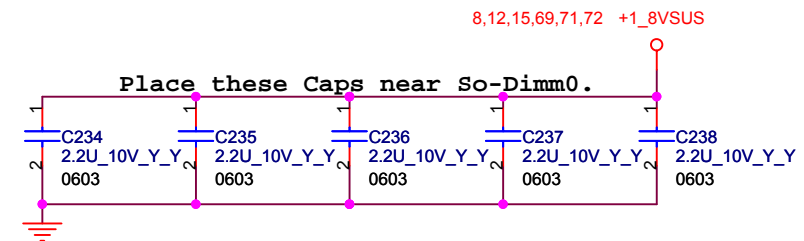
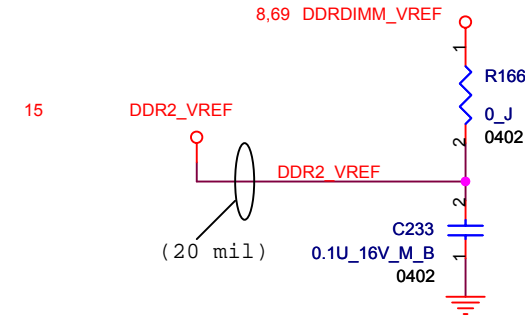
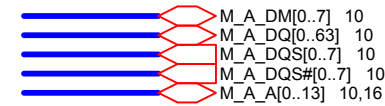
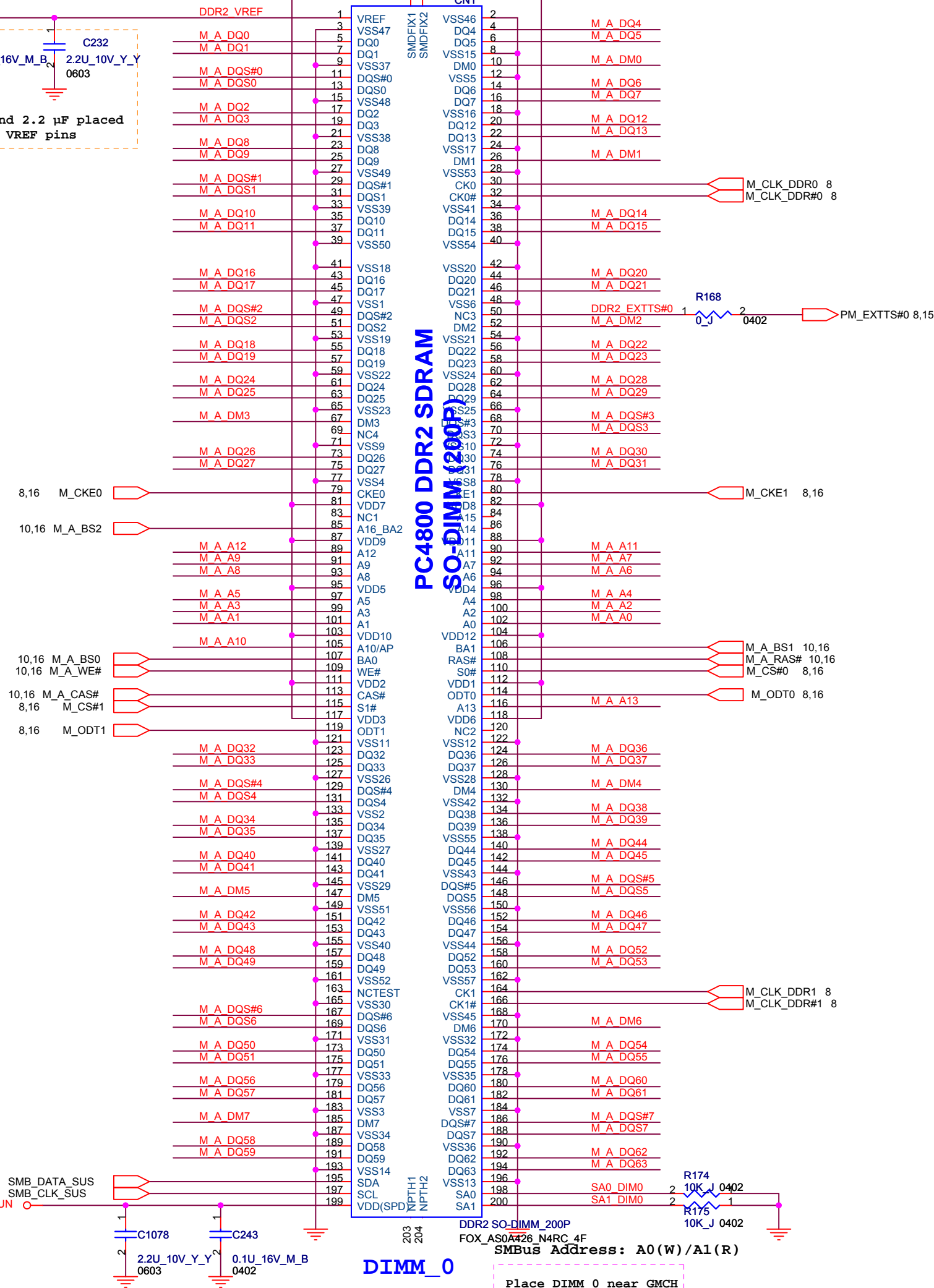
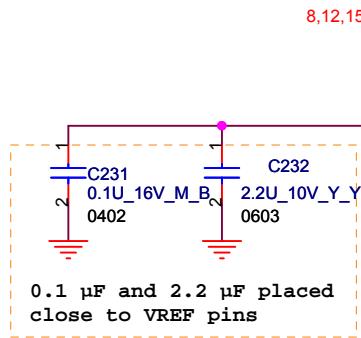
8 MCH_CFG_19 ◀ 1 30MIL TP558

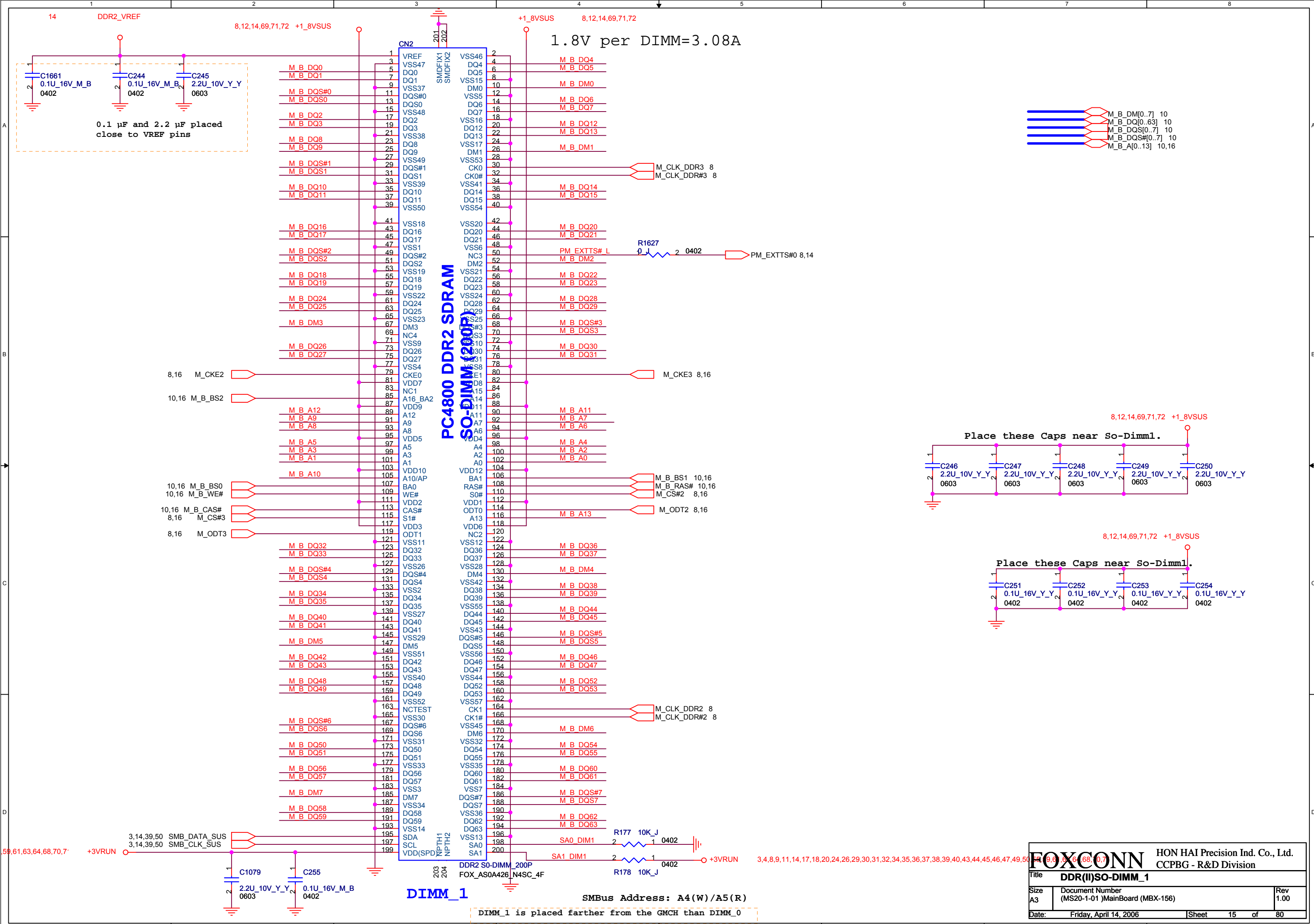
MCH_CFG_20 (PCIE Backward Interpoerability mode)	Low = Only SDVO or PCIE x1 is operational (defaults)) High = SDVO and PCIE x1 are operating simultaneously via the PEG port
---	--

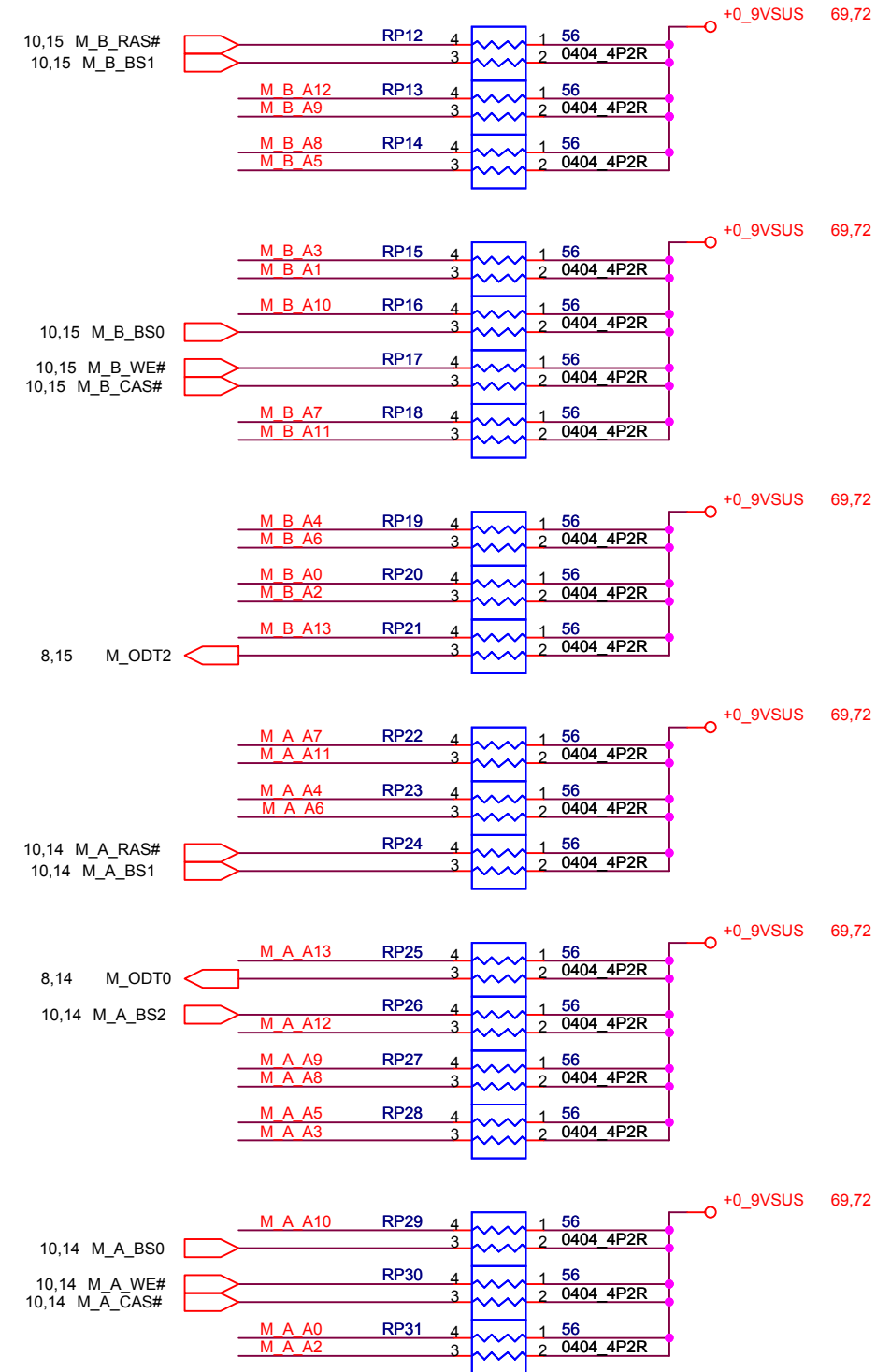
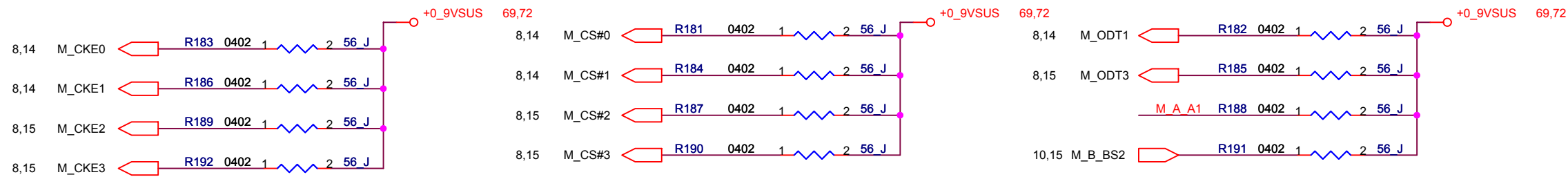
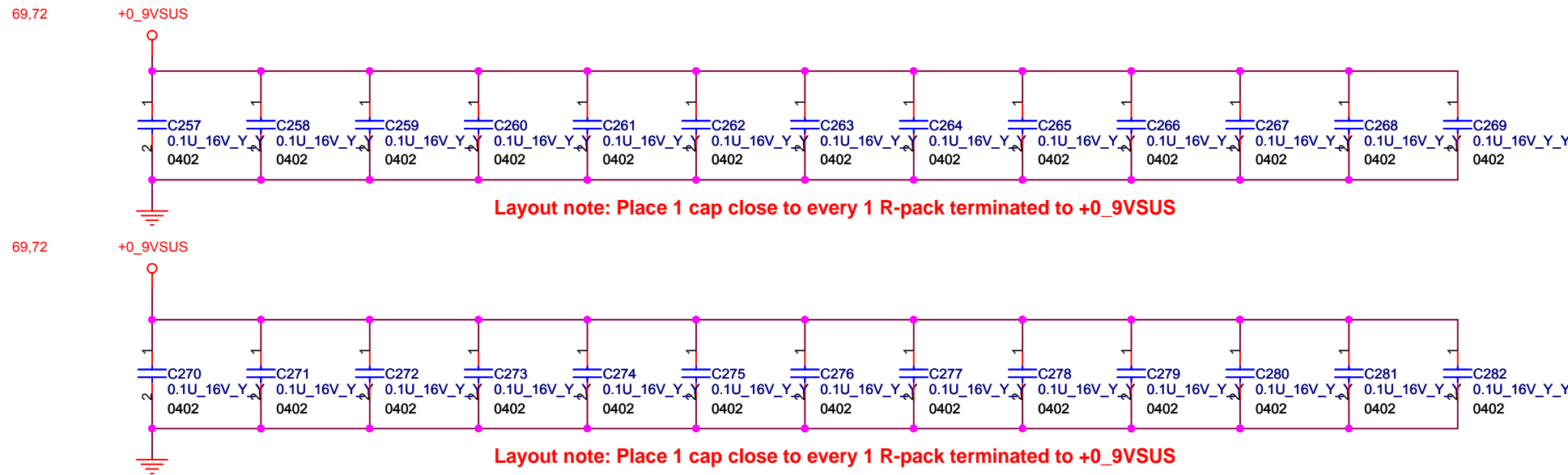
8 MCH_CFG_20 ◀ 1 30MIL TP561

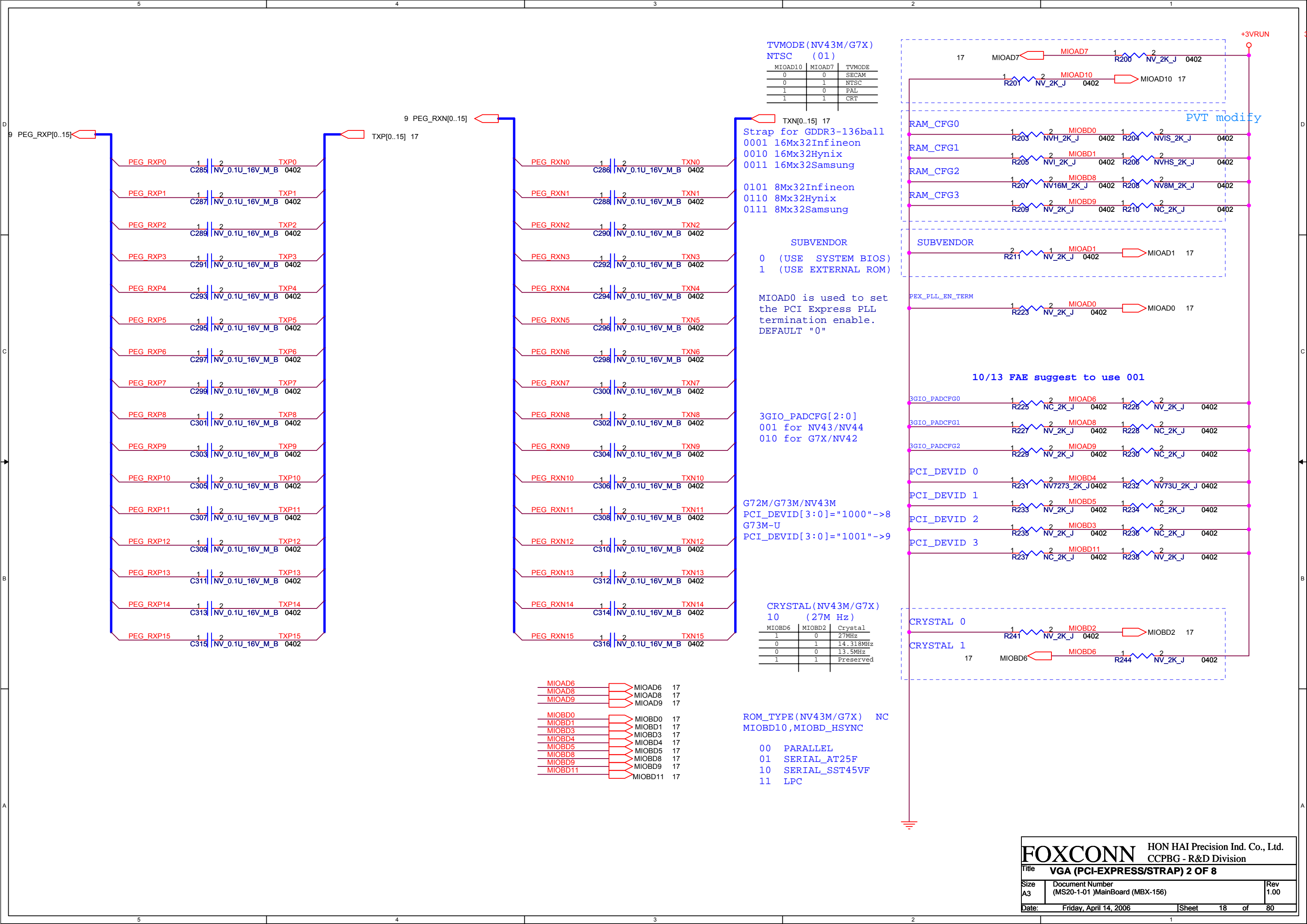
Layout Noe:
Location of all MCH_CFG strap resistors needs to be close to trace to minimize stub

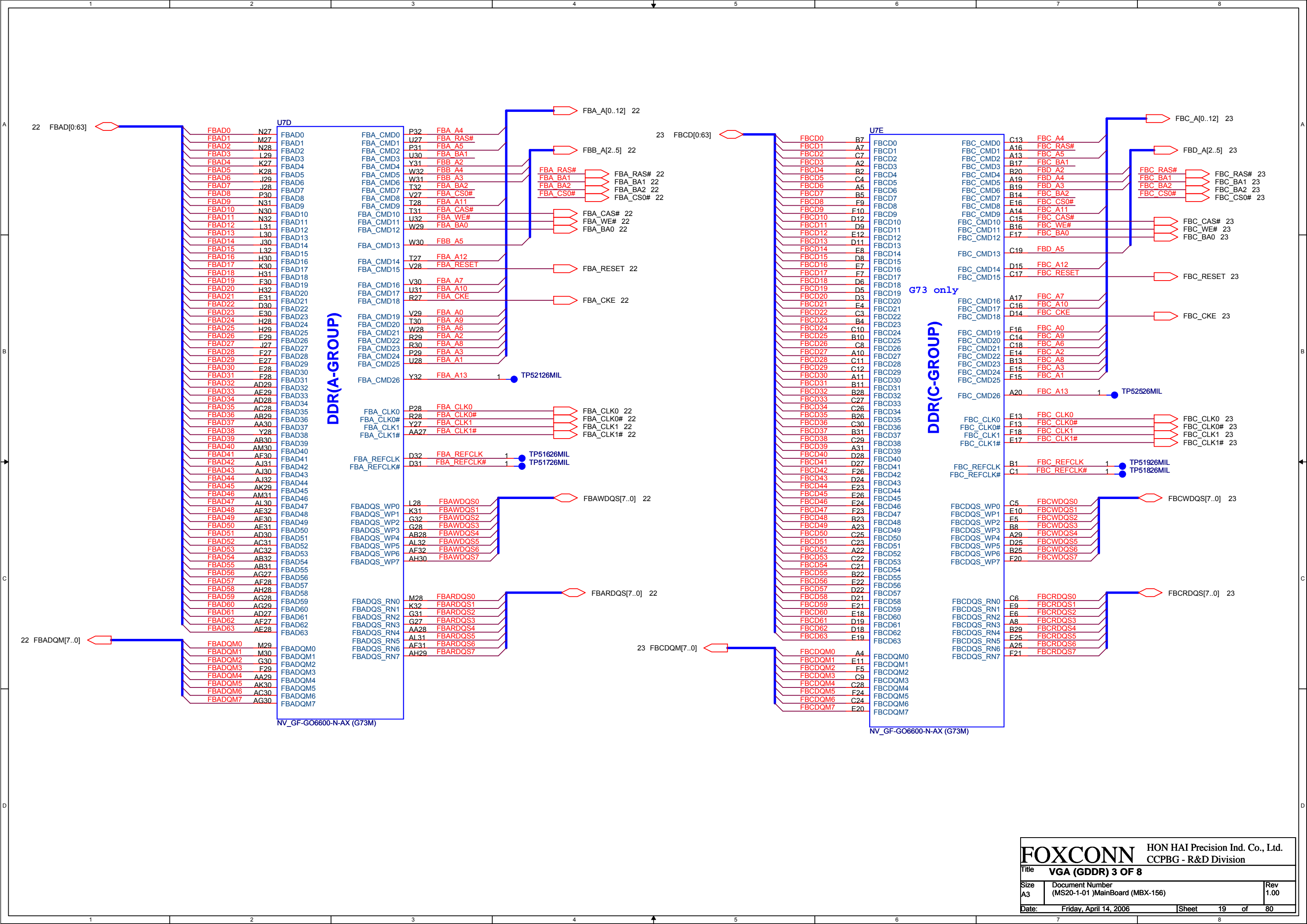


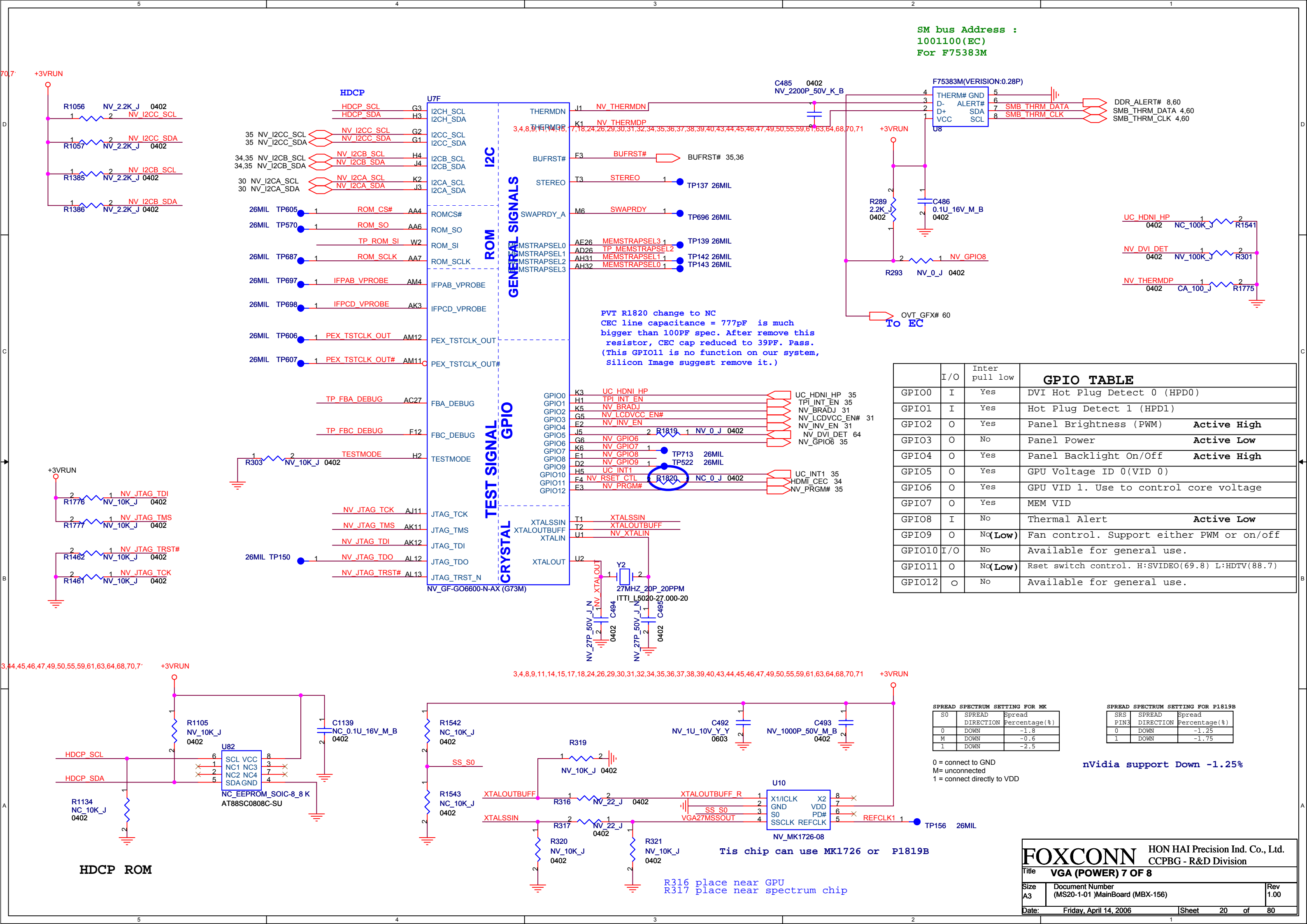


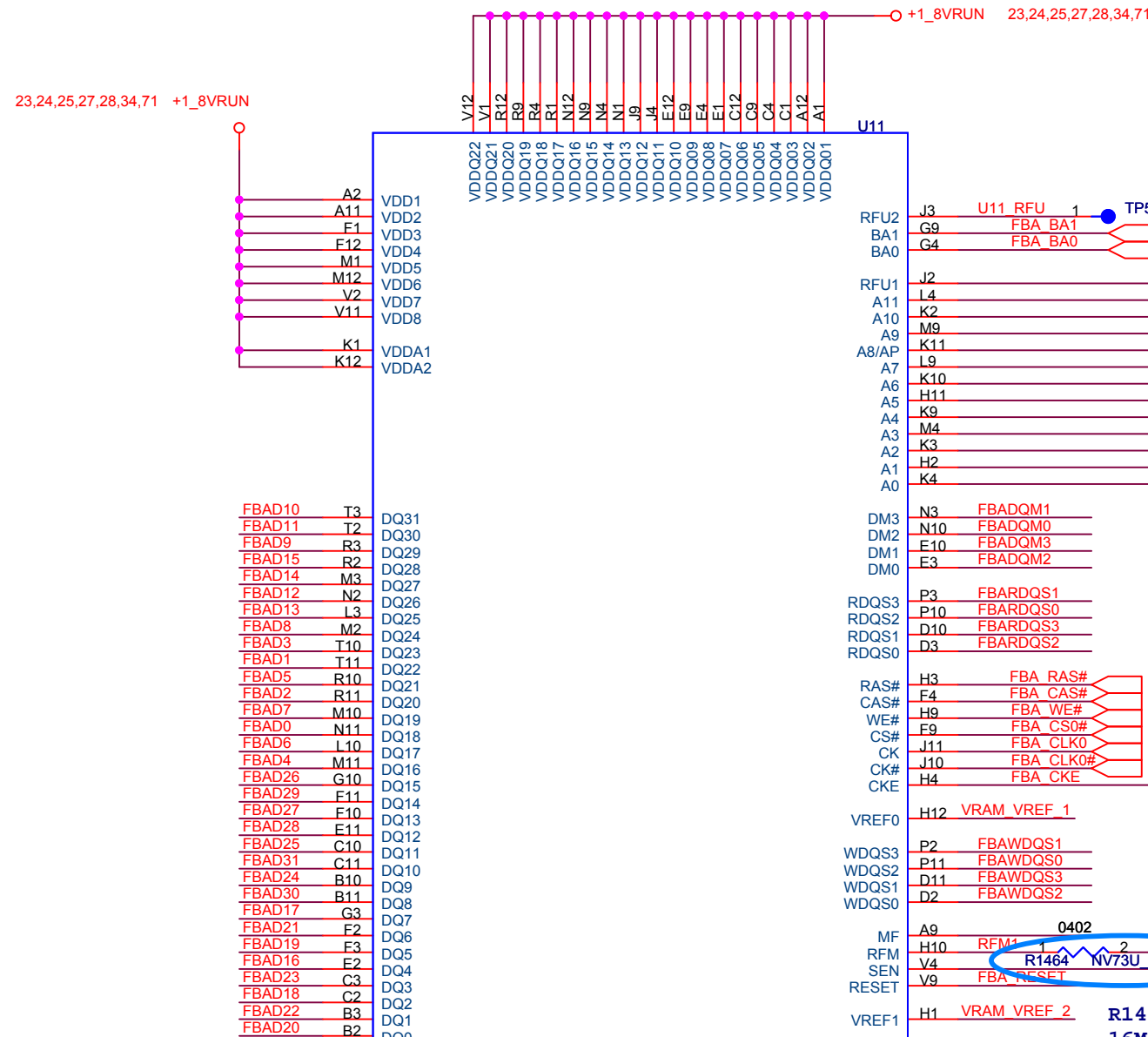






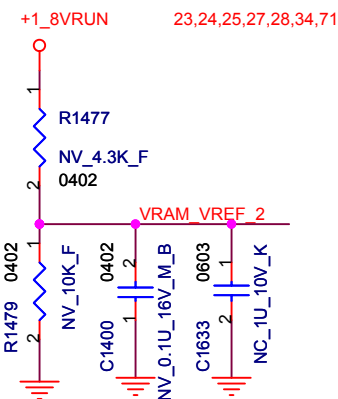
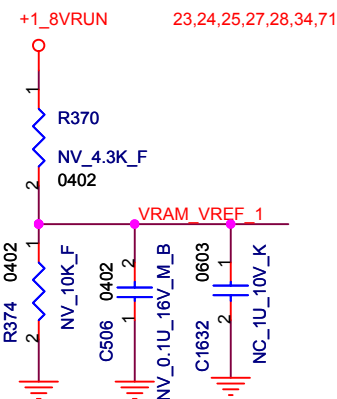






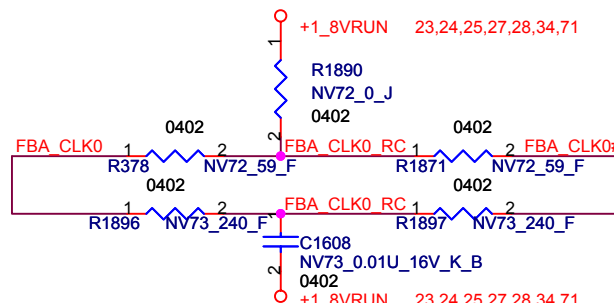
R1397(120 ohm-360 ohm)
240 ohm --> Output impedance 40 ohm

VRAM_VREF is 70%FBVDDQ for GDDR3 1.26V



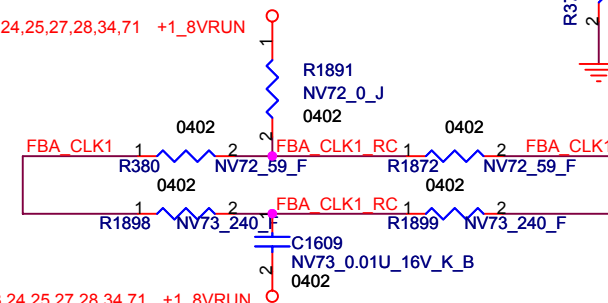
PVT modify

FAE suggestion on 10/26
Close to VRAM

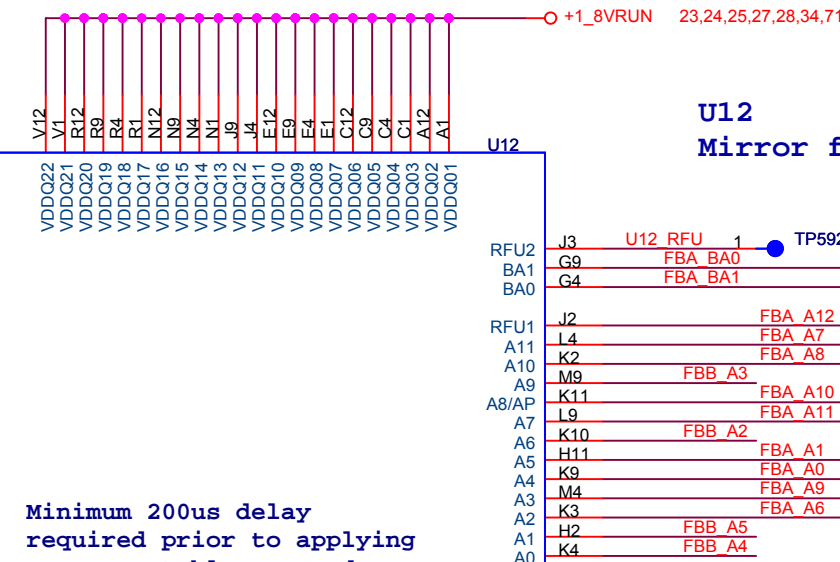


12/20 Nvidia update

	DDR3 (G72M)	DDR3 (G73M)
R378,R380 R1871,R1872	60 ohm	240 ohm
R,C 1890 R,C 1891	0 ohm	0.01uF



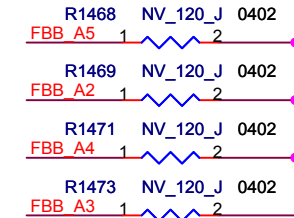
Minimum 200us delay
required prior to applying
any executable command
after stable power and clock.



U12
Mirror function on

PVT modify

R1463
16M stuff
8M no stuff

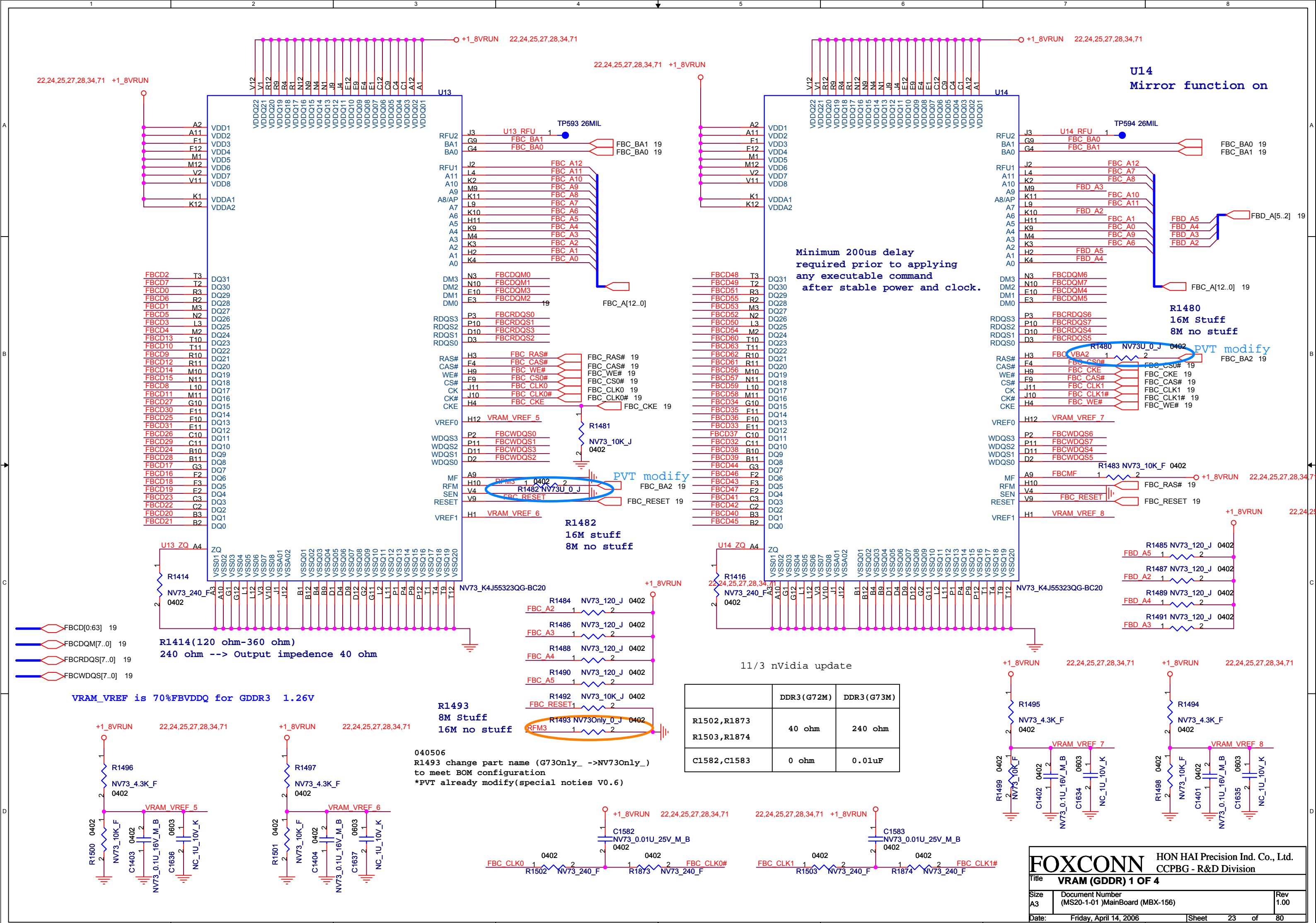


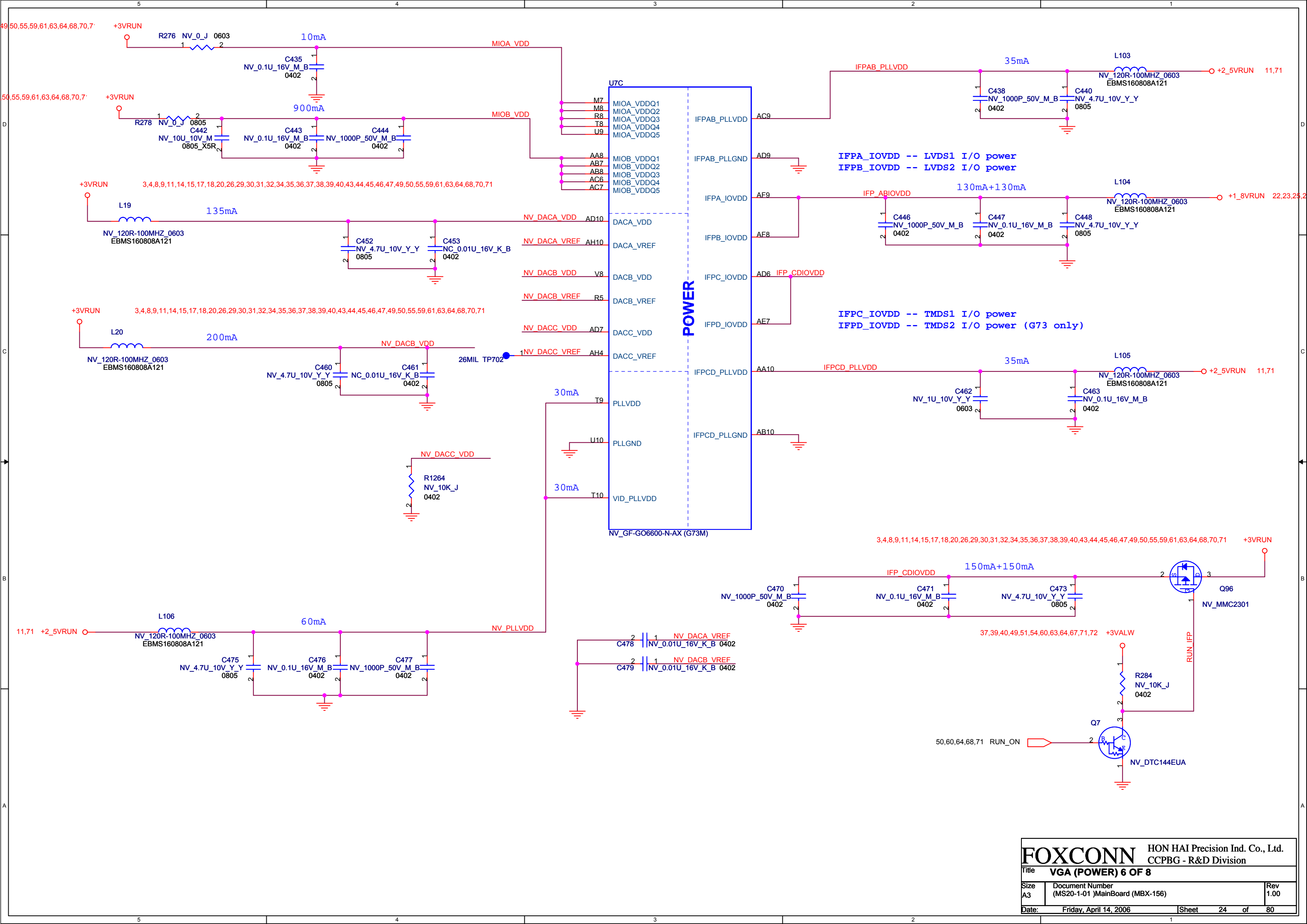
FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title VRAM (GDDR) 1 OF 4

Size A3 Document Number (MS20-1-01) MainBoard (MBX-156) Rev 1.00

Date: Friday, April 14, 2006 Sheet 22 of 80





U7



	DDR1	DDR3 (G72M)	DDR3 (G73M)
FBCAL_PD_VDDQ	40 ohm	60 ohm	50 ohm
FBCAL_PU_GND	30 ohm	40 ohm	40 ohm
FBCAL_TERM_GND	NC	40 ohm	40 ohm

25,72,73

25,72,73

25,72,73

25,72,73

72,73

2,4,7,49,50,55,59,61,63,64,68,70,71

G3 design guide require
that PEX_IOVDD/Q directly connect to
PEX_VDD on page 16.

U7B

AD23 PEX_IOVDD0
AF24 PEX_IOVDD1
AF23 PEX_IOVDD2
AG25 PEX_IOVDD3
AG24 PEX_IOVDD4
AG25 PEX_IOVDD5

AC16 PEX_IOVDDQ0
AC17 PEX_IOVDDQ1
AC21 PEX_IOVDDQ2
AC22 PEX_IOVDDQ3
AE18 PEX_IOVDDQ4
AE21 PEX_IOVDDQ5
AE22 PEX_IOVDDQ6
AE12 PEX_IOVDDQ7
AE18 PEX_IOVDDQ8
AF21 PEX_IOVDDQ9
AF22 PEX_IOVDDQ10

AF15 PEX_PLLAVDD

AE15 PEX_PLLDVDD

AE16 PEX_PLLGND

P20 VDD_LP1
T20 VDD_LP2
T23 VDD_LP3
U20 VDD_LP4
U23 VDD_LP5
W20 VDD_LP6

AC11 VDD33_0
AC12 VDD33_1
AC24 VDD33_2
AD24 VDD33_3
AE11 VDD33_4
AE12 VDD33_5
H7 VDD33_6
J7 VDD33_7
K7 VDD33_8
L10 VDD33_9
L7 VDD33_10
L8 VDD33_11
M10 VDD33_12

55

HSPDIF

26MIL TP624
26MIL TP626
26MIL TP628
26MIL TP629

26MIL TP635
26MIL TP634
26MIL TP636
26MIL TP637

TP NFNC1 AG12
TP NFNC2 AH13
HSPDIF J6
NFNC4 B32
NFNC5 AM9
NFNC6 AM8
NFNC7 Y30
TP NFNC8 AC26
NFNC9 U3
NFNC10 V3
NFNC11 U6
NFNC12 U5

NV_GF-GO6600-N-AX (G73M)

POWER

VDD0 K16
VDD1 K17
VDD2 N13
VDD3 N14
VDD4 N16
VDD5 N17
VDD6 N19
VDD7 N20
VDD8 P13
VDD9 P14
VDD10 P16
VDD11 P17
VDD12 P19
VDD13 R16
VDD14 R17
VDD16 T14
VDD17 T15
VDD18 T18
VDD19 T19

VDD20 U13
VDD21 U14
VDD22 U15
VDD23 U18
VDD24 U19
VDD25 V16
VDD26 V17
VDD27 W13
VDD28 W14
VDD29 W16

VDD30 W17
VDD31 W19
VDD32 Y13
VDD33 Y14
VDD34 Y16
VDD35 Y17
VDD36 Y19
VDD37 Y20

NC13 U4
NC14 V4
NC15 V6
NC16 C20
NC17 D1
NC18 W3
NC19 V1
NC20 Y5
NC21 W1
NC22 W4
NC23 W5
NC24 V5
NC25 Y6
NC26 F6
NC27 G8
NC28 G23
NC29 A28
NC30 E1
NC31 A26

NFNC13 1 TP614 26MIL
NFNC14 1 TP613 26MIL
NFNC15 1 TP616 26MIL
NFNC16 1 TP615 26MIL
NFNC17 1 TP618 26MIL
NFNC18 1 TP617 26MIL
NFNC19 1 TP620 26MIL
NFNC20 1 TP622 26MIL
NFNC21 1 TP623 26MIL
NFNC22 1 TP625 26MIL
NFNC23 1 TP627 26MIL
NFNC24 1 TP631 26MIL
NFNC25 1 TP630 26MIL
NFNC26 1 TP633 26MIL
TP FBC PLLVDD 1 TP586 26MIL
FBA PLLVDD 1 TP587 26MIL
FB VREF2 1 TP590 26MIL
STRAP 1
TESTMEMCLK 1 2

R1544 NV72_10K_J 0402

G73M Pin A26-NC
G72M Pin A26 need stuff R305 10K

8mA(Frame Buffer Analog Power)

NV_PLLAVDD
NV_0.1U_16V_Y_Y C1191 0402
NV_4.7U_10V_Y_Y C1192 0805
NV_120R-100MHZ_0603 EBMS160808A121
NC_1000P_50V_K_B C1216 0402

16.25A(Internal logic core power)

NV_0.1U_16V_M_B C329 0402
NV_0.1U_16V_M_B C330 0402
NV_0.1U_16V_M_B C331 0402

CRB circuit

NV_0.01U_16V_K_B C1193 0402
NV_0.01U_16V_M_B C333 0402
NV_0.01U_16V_M_B C334 0402
NV_0.01U_16V_M_B C335 0402

NV_0.1U_16V_M_B C340 0402
NV_0.1U_16V_M_B C341 0402
NV_0.1U_16V_M_B C342 0402

NV_1000P_50V_M_B C356 0402
NV_1000P_50V_M_B C357 0402
NV_1000P_50V_M_B C358 0402

NV_22U_6.3V_M_B C362 0805
NV_22U_6.3V_M_B C363 0805
NV_22U_6.3V_M_B C364 0805

2006.4.11

NV_VDD on G73M-U power noise issue,modify BOM configuration,
(1)G73M-U (H) C352,C362,C363,C364
on 22uF / X5R / 0805(1C-2B70226-M100)
(2)G72 (L) / G73 (M) C352,C362,C363,C364
on 10uF / X5R / 0805(1C-2B70106-M100)

FOXCONN

HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title VGA (GDDR/I2C/ROM) 4 OF 8

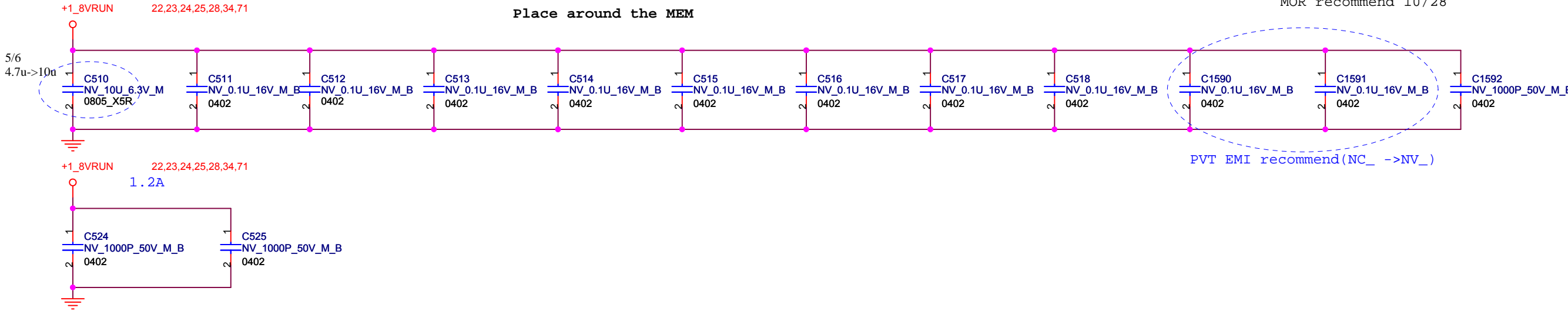
Size A3 Document Number (MS20-1-01)MainBoard (MBX-156) Rev 1.00

Date: Friday, April 14, 2006 Sheet 26 of 80

Decoupling for Tright MEMORY

Place around the MEM

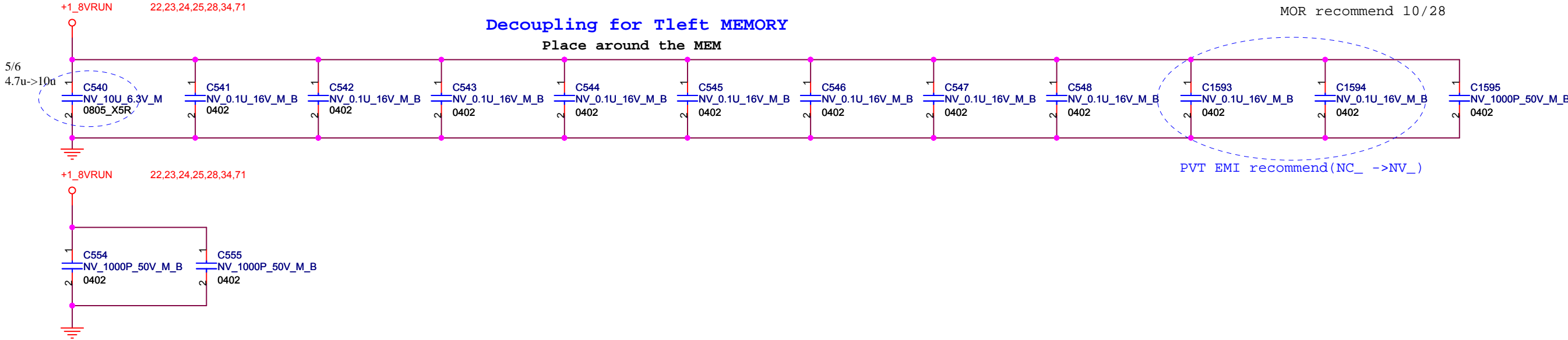
MOR recommend 10/28



Decoupling for Tleft MEMORY

Place around the MEM

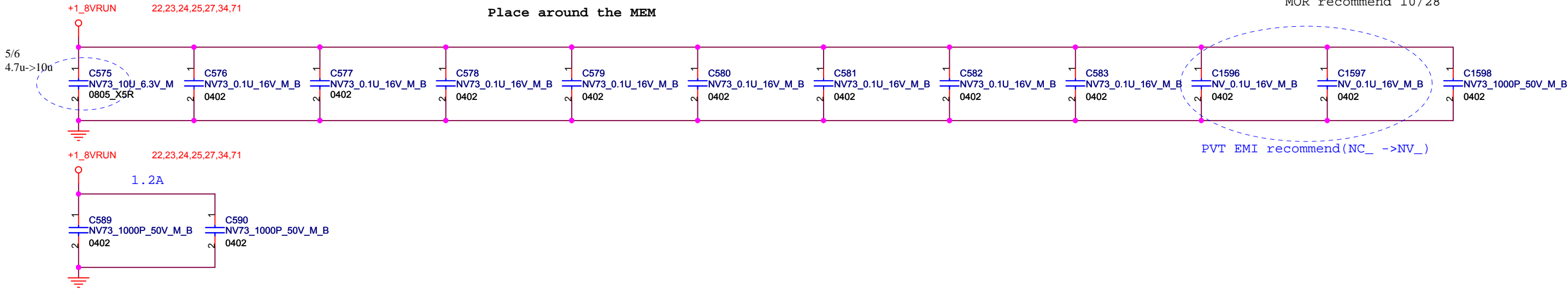
MOR recommend 10/28



Decoupling for Bright MEMORY

Place around the MEM

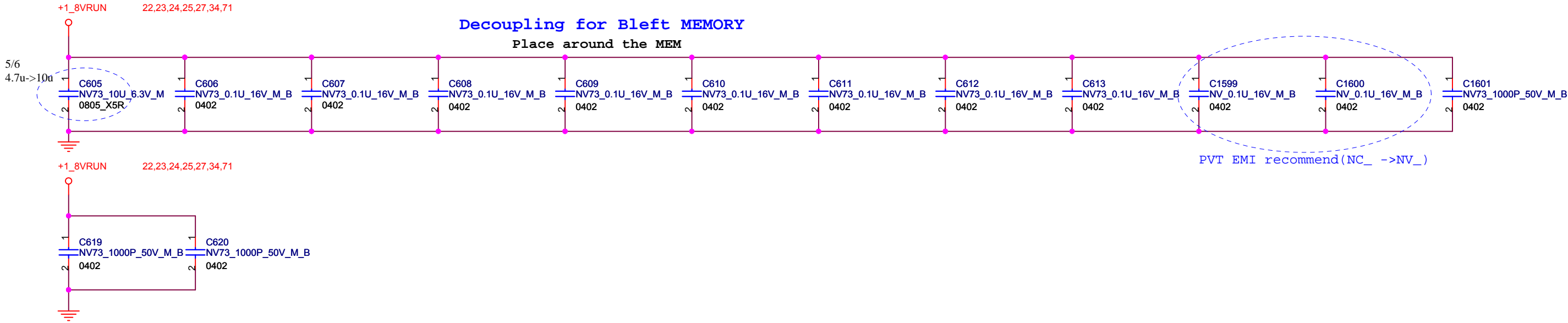
MOR recommend 10/28



Decoupling for Bleft MEMORY

Place around the MEM

PVT EMI recommend (NC_ -> NV_)

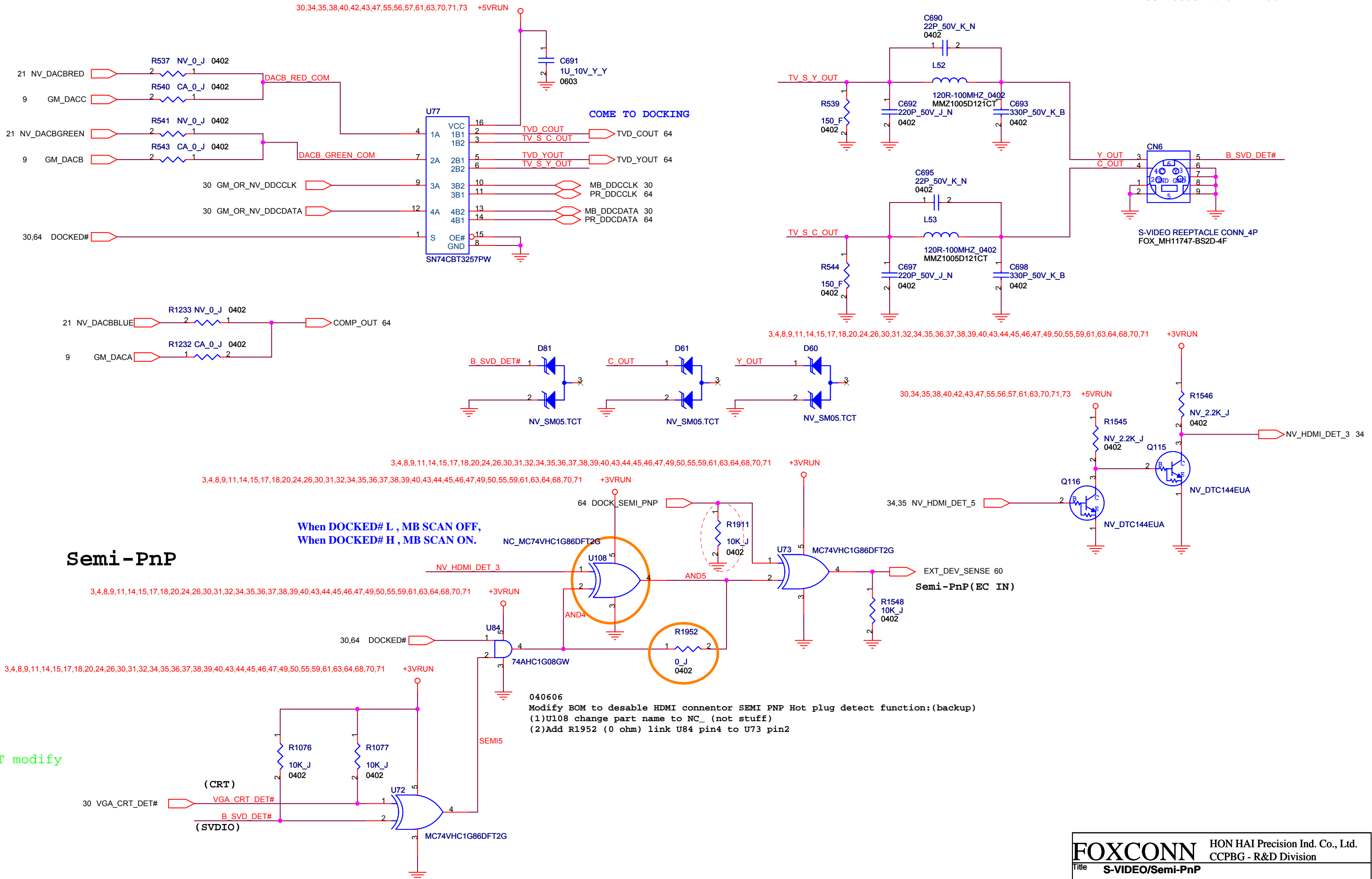


S-VIDEO ANALOG SWITCH

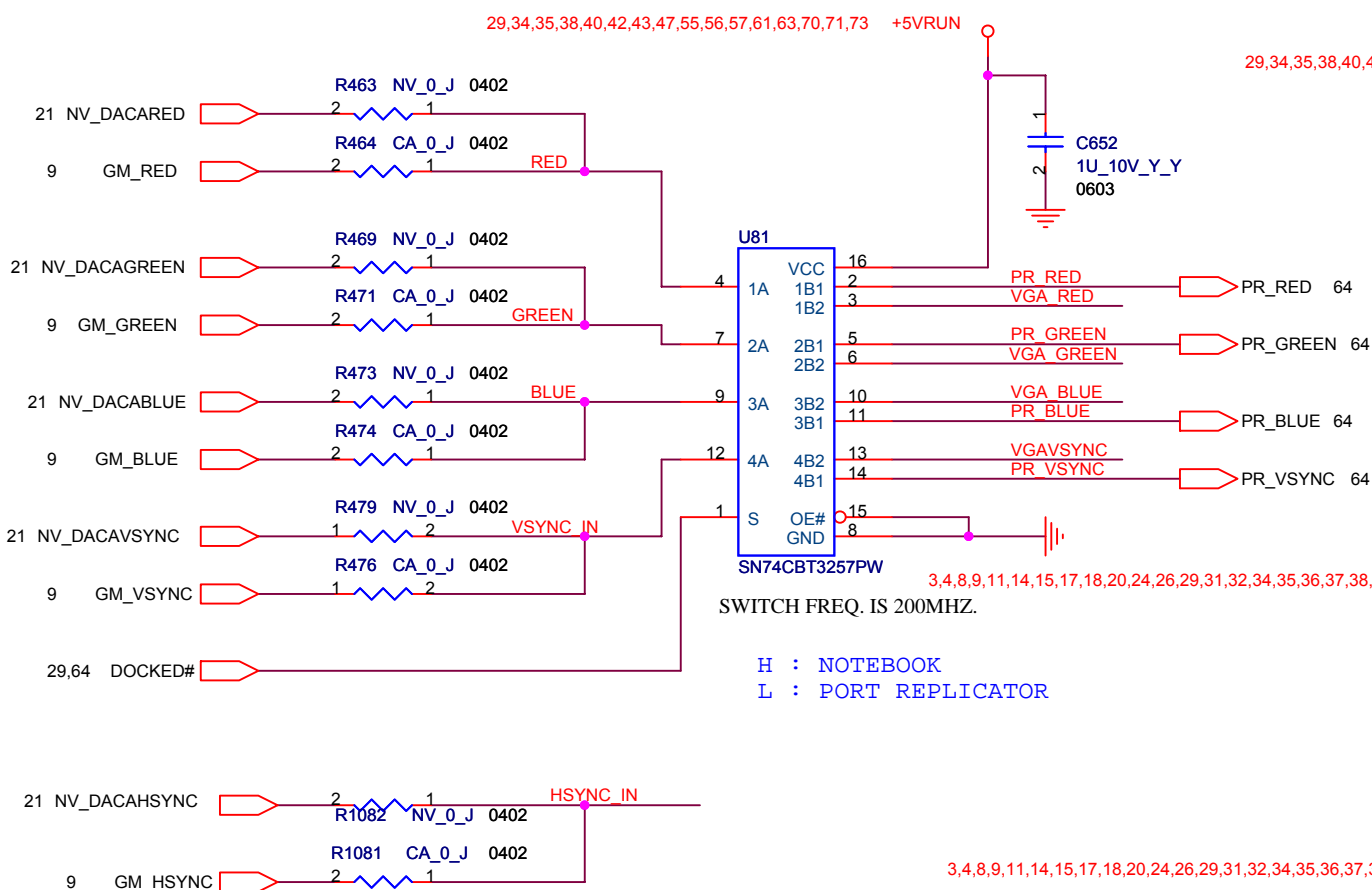
H : S-VIDEO&CVBS
L : PORT REPLICATOR

S-VIDEO

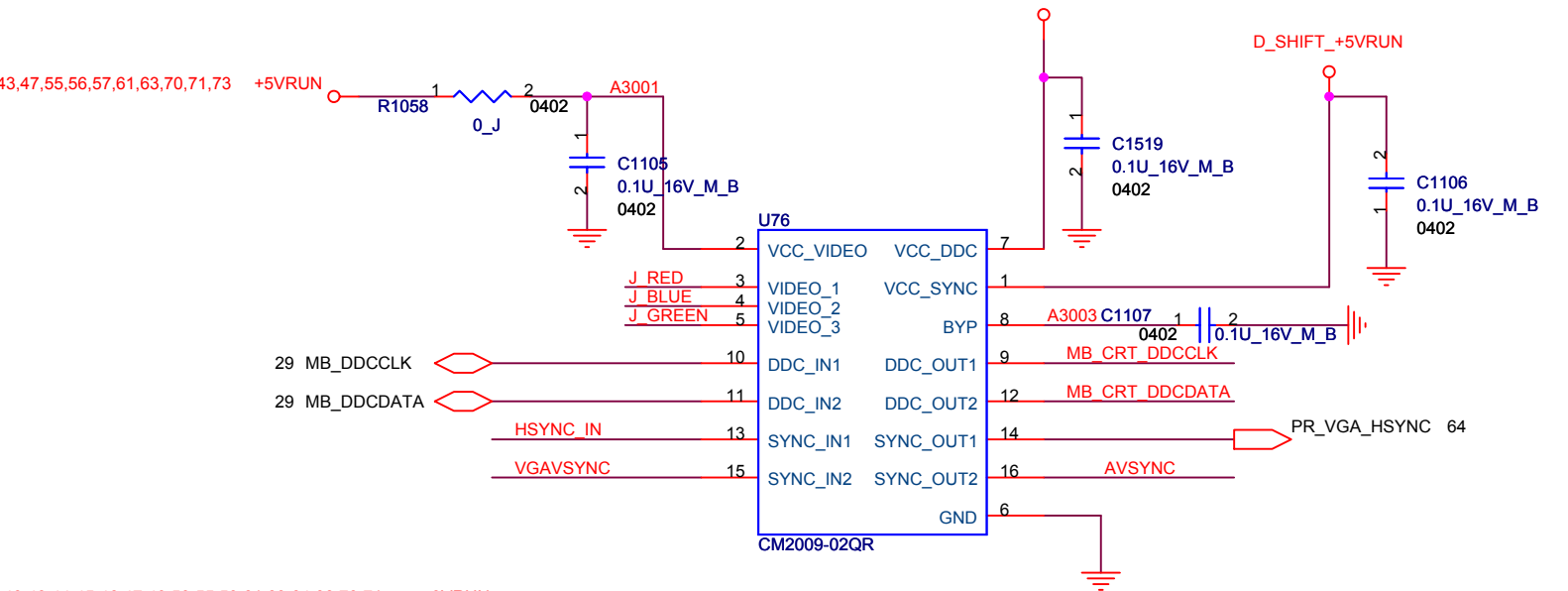
These compoent close to S-Video connector within 700 mil



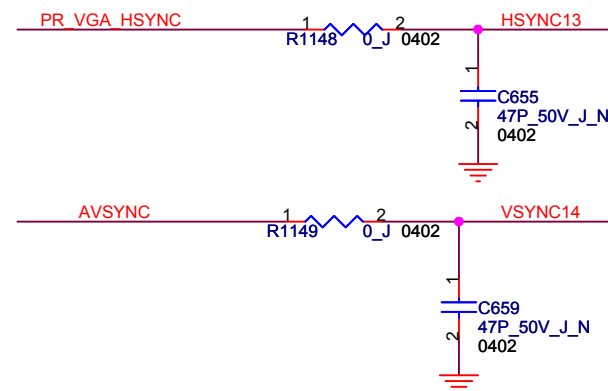
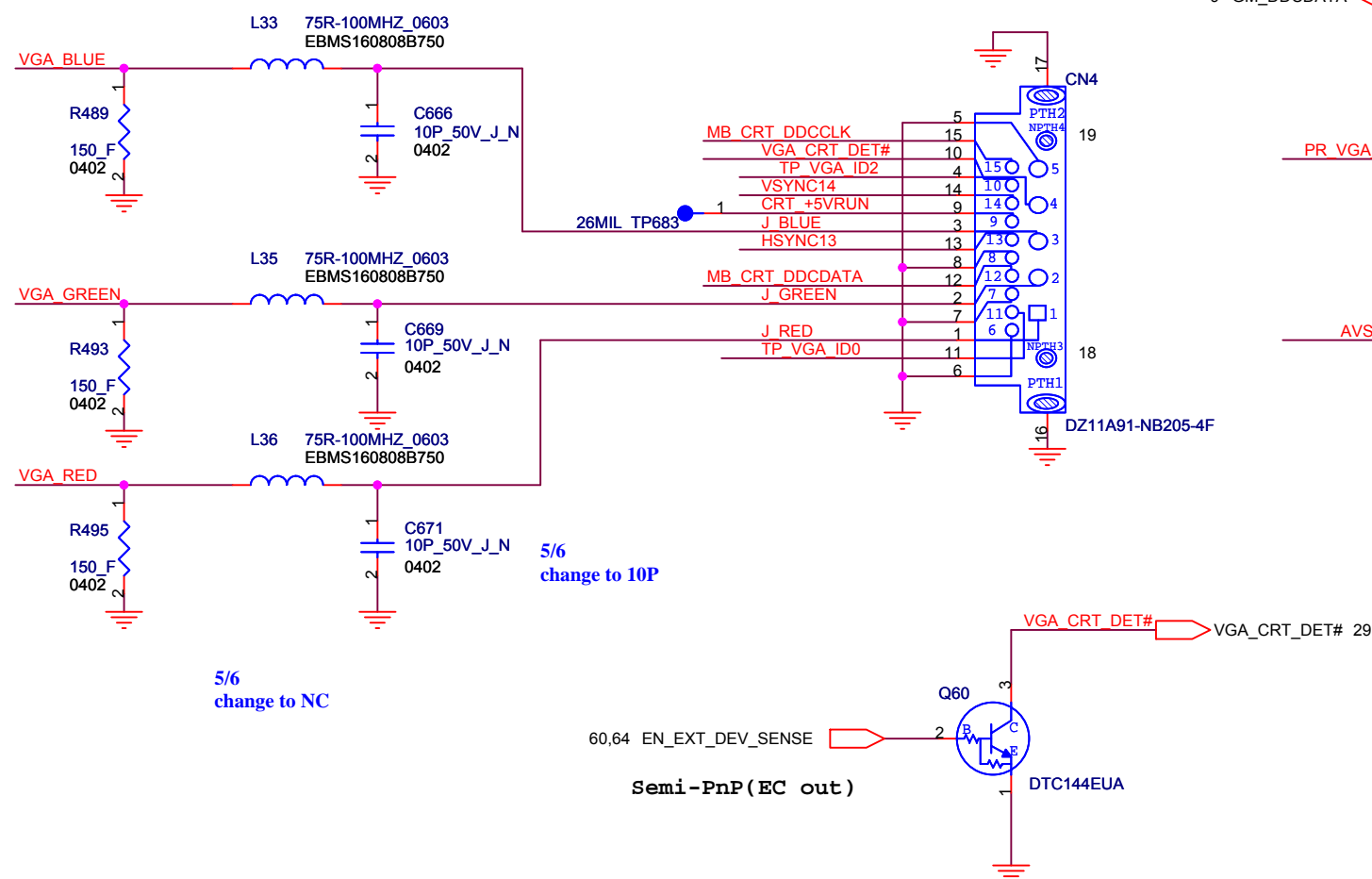
CRT ANALOG SWITCH



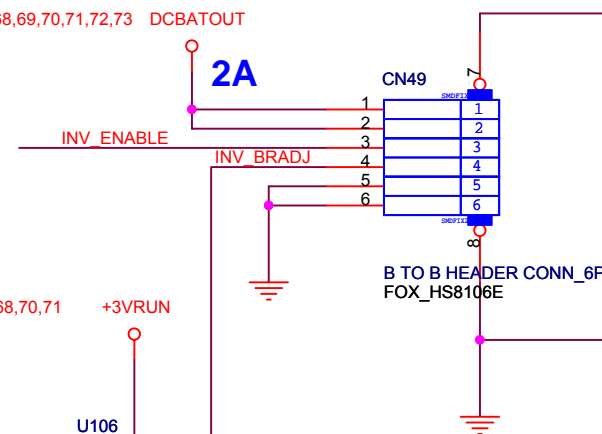
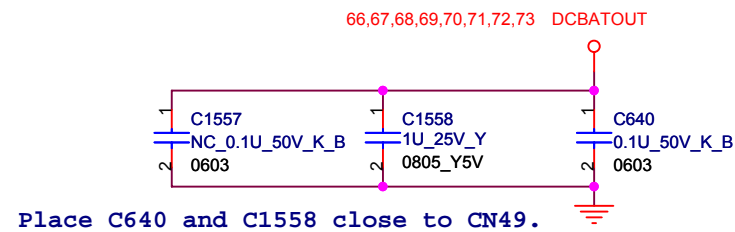
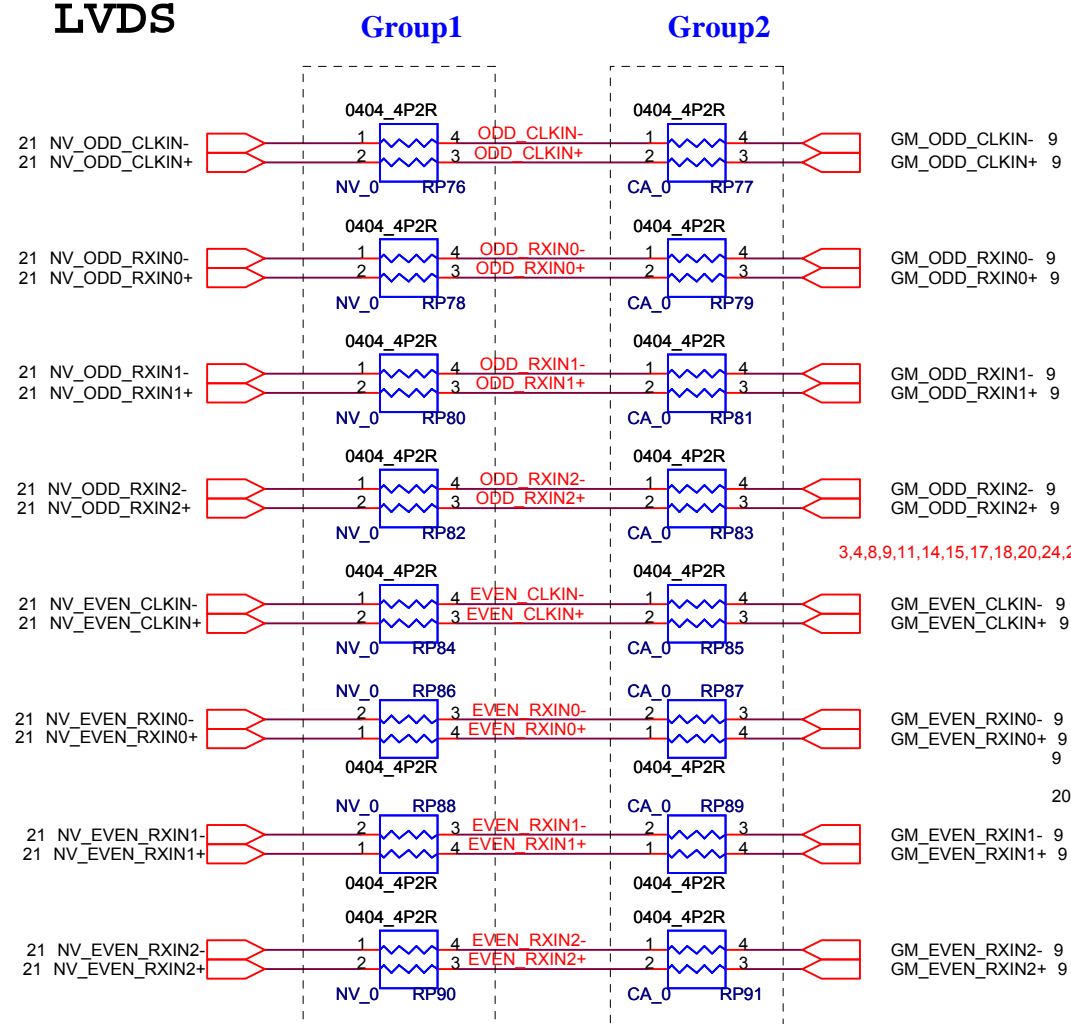
3,4,8,9,11,14,15,17,18,20,24,26,29,31,32,34,35,36,37,38,39,40,43,44,45,46,47,49,50,55,59,61,63,64,68,70,71 +3VRUN



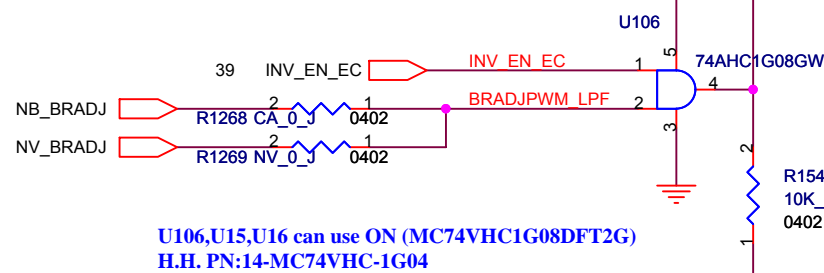
CRT CONNECTOR



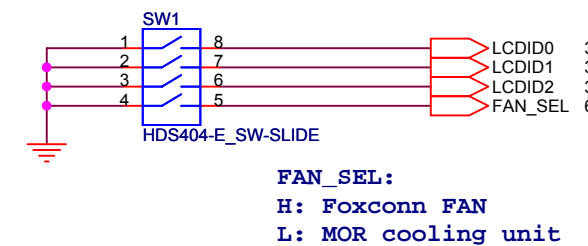
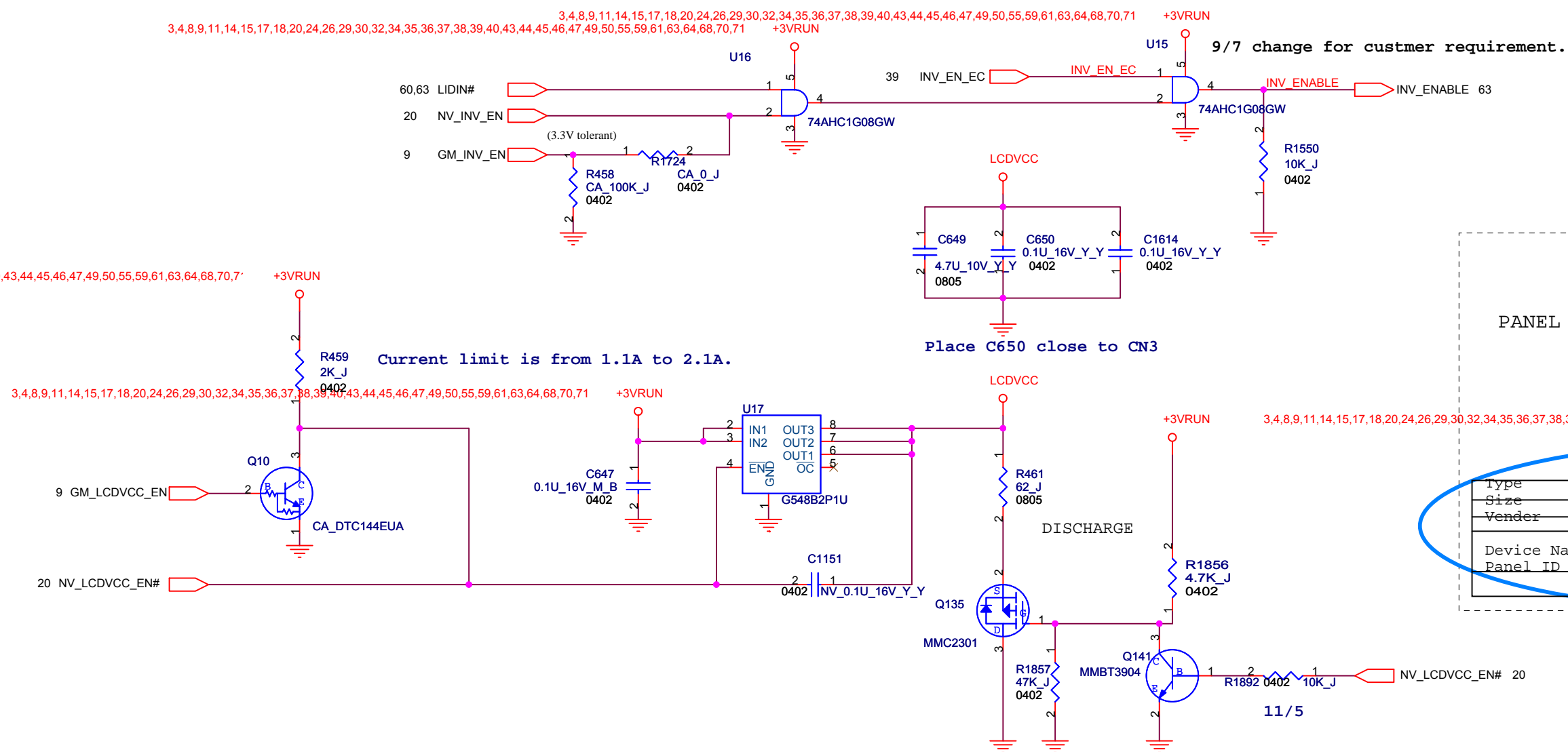
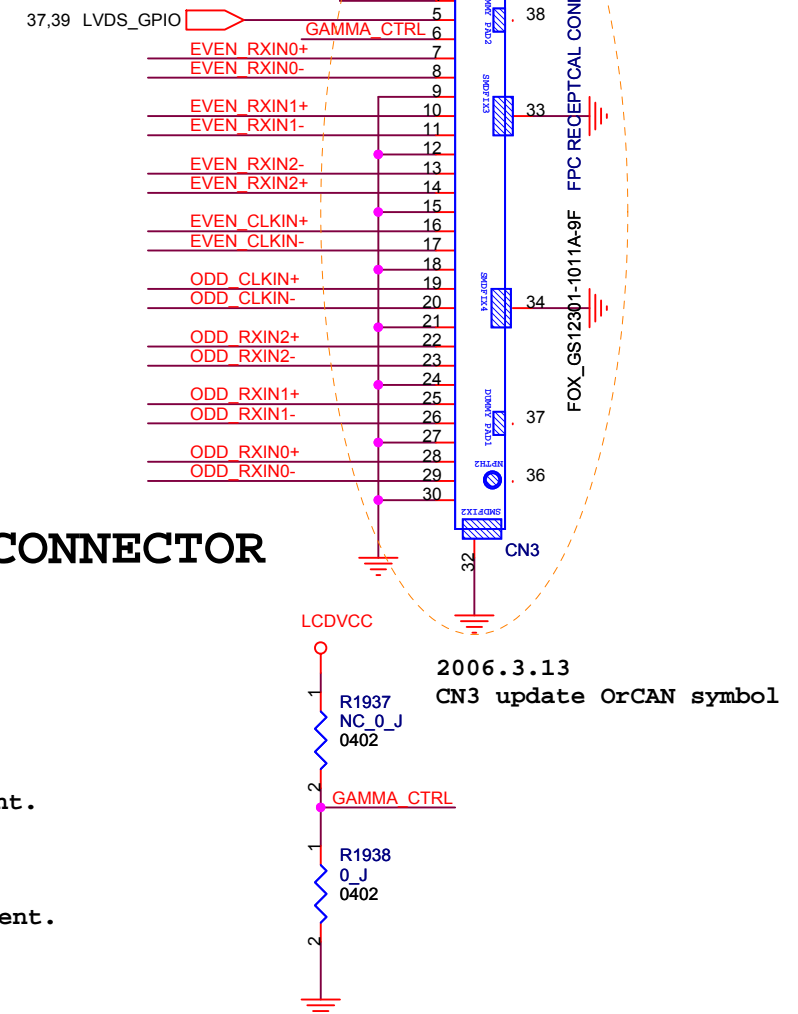
LVDS



INVERTER CONNECTOR



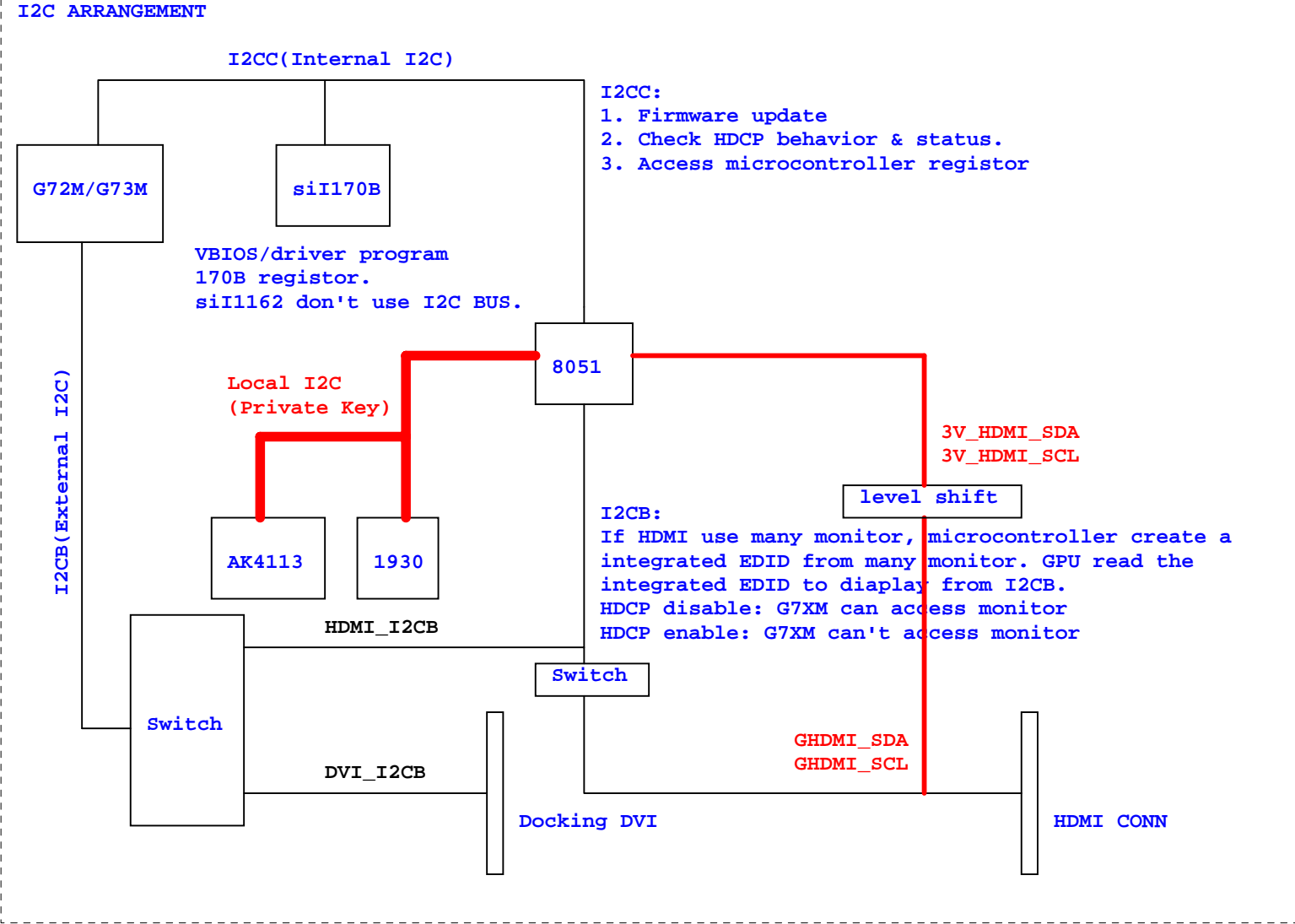
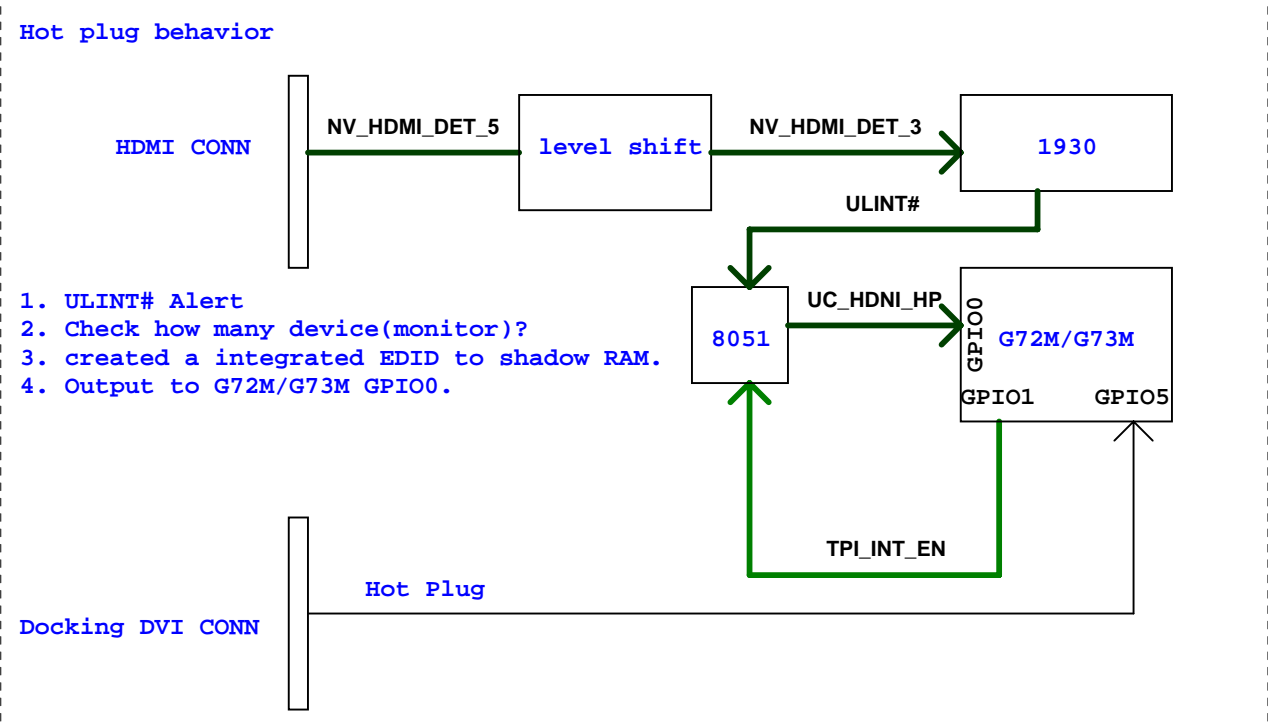
9/7 change for customer requirement.

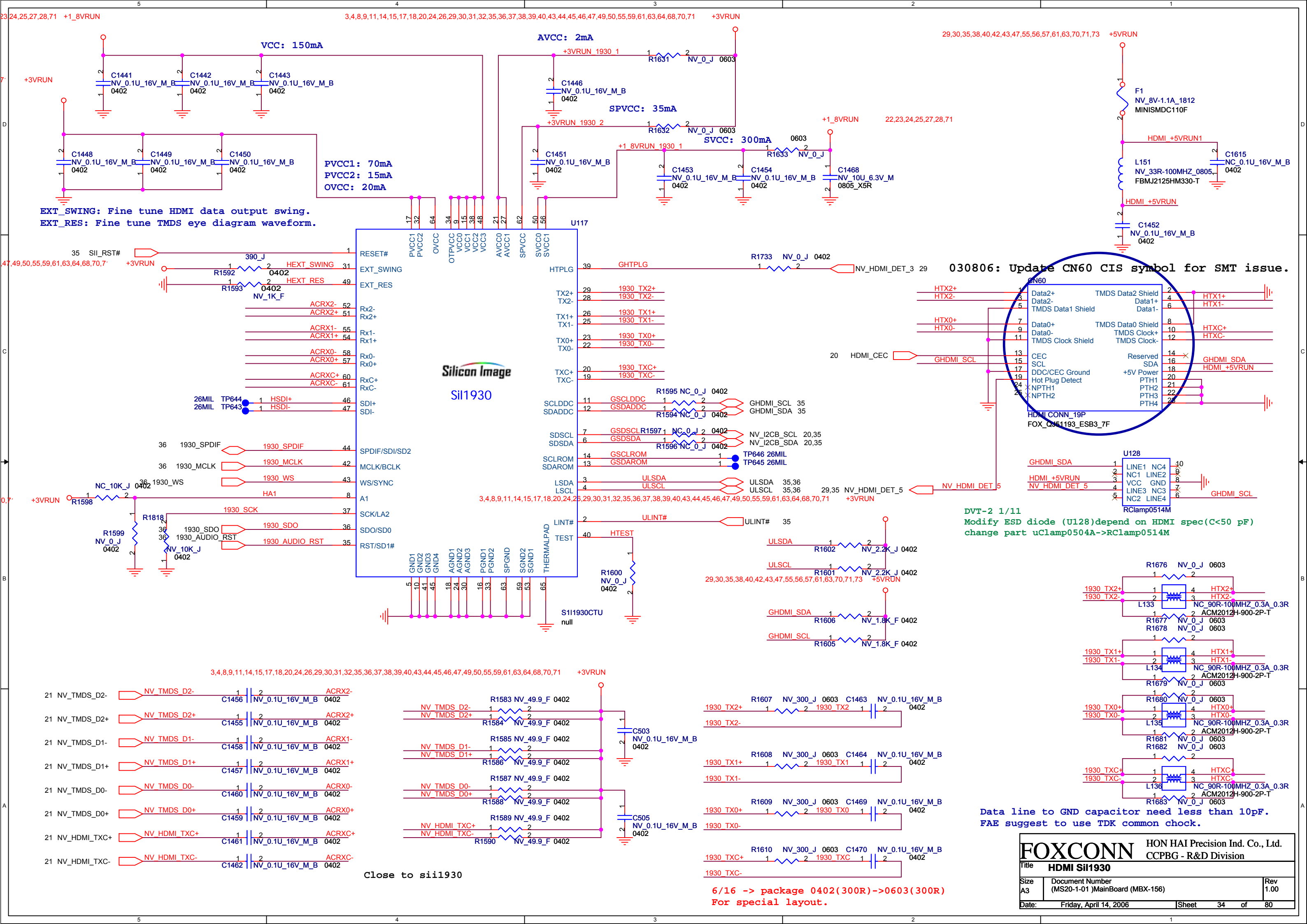


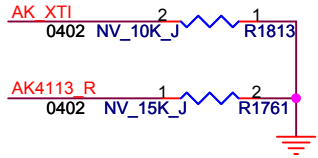
Type	WXGA+	WXGA+	WUXGA
Size	17" wide	17" wide	17" wide
Vender	LG.PHILIPS	LG.PHILIPS	SHARP
Device Name	LP171WF7-TLA1	LP171WX2-A4K3	LQ170MILA04
Panel ID Check[3..0]	2 Lamps 0001	1 Lamps 0010	2 Lamps 0100

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title LVDS			
Size A3	Document Number (MS20-1-01) MainBoard (MBX-156)		Rev 1.00
Date:	Friday, April 14, 2006	Sheet	31 of 80

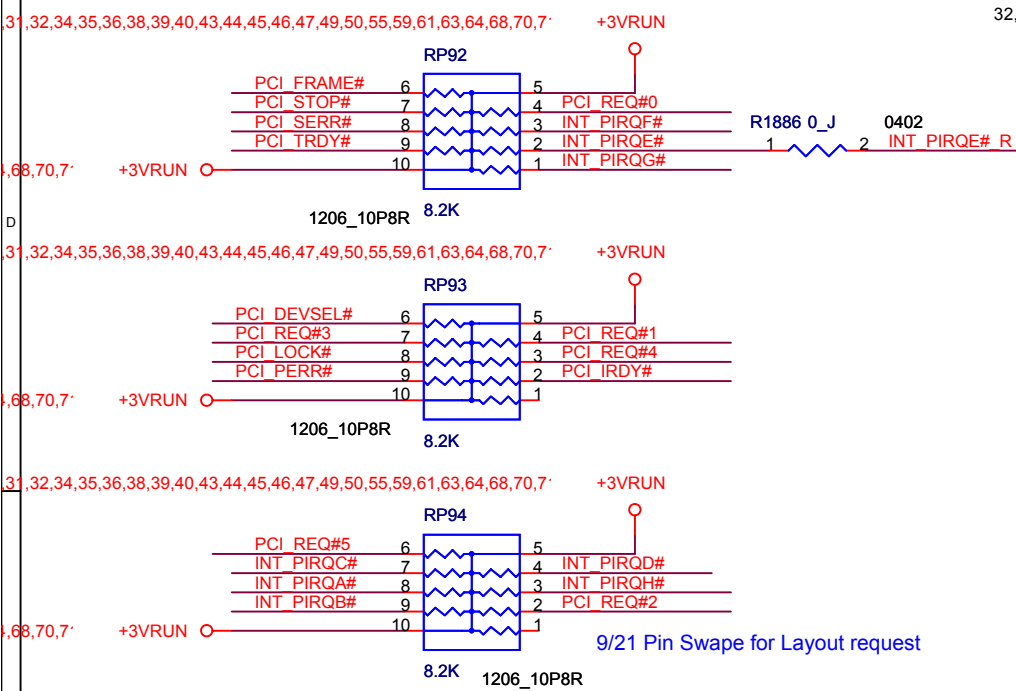
Hot plug behavior & I2C ARRANGEMENT block diagram







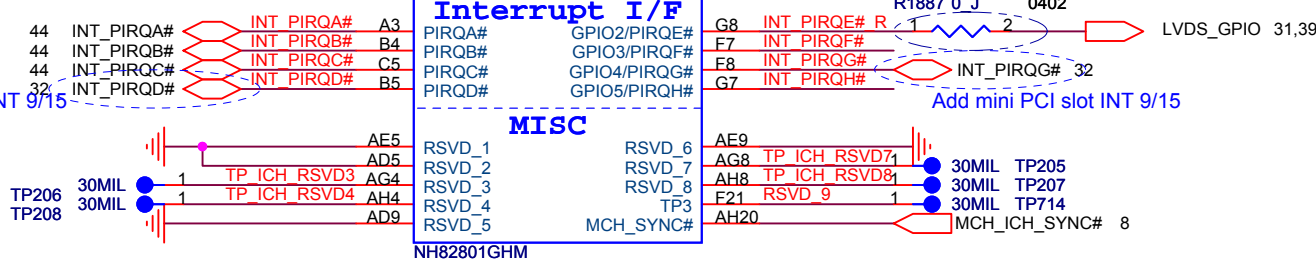
FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
MINI-PCI CONN.	
Size 3	Document Number (MS20-1-01)MainBoard (MBX-156)
Date: Friday, April 14, 2006	Sheet 36 of 80
Rev 1.00	



PCI Pullups

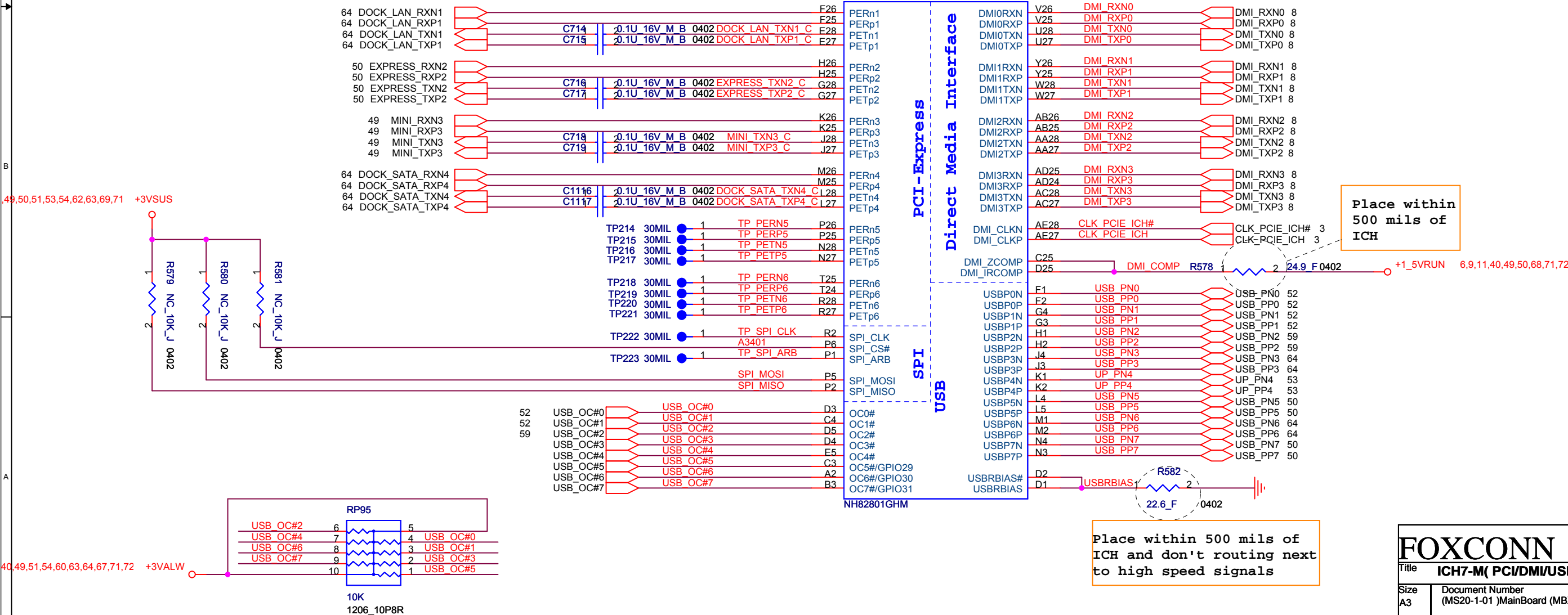
9/21 Pin Swape for Layout request

Add mini PCI slot INT 9/15



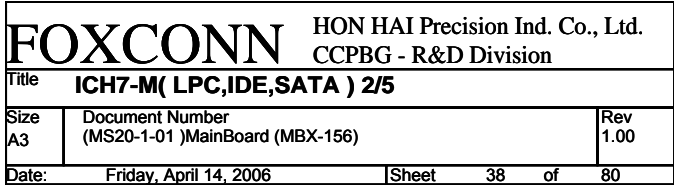
Strap for Boot-BIOS

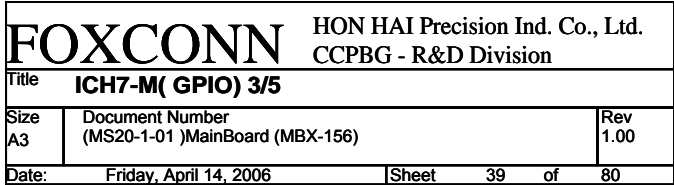
	GNT5#	GNT4#
LPC(Default)	Hi	Hi
PCI	Hi	LOW

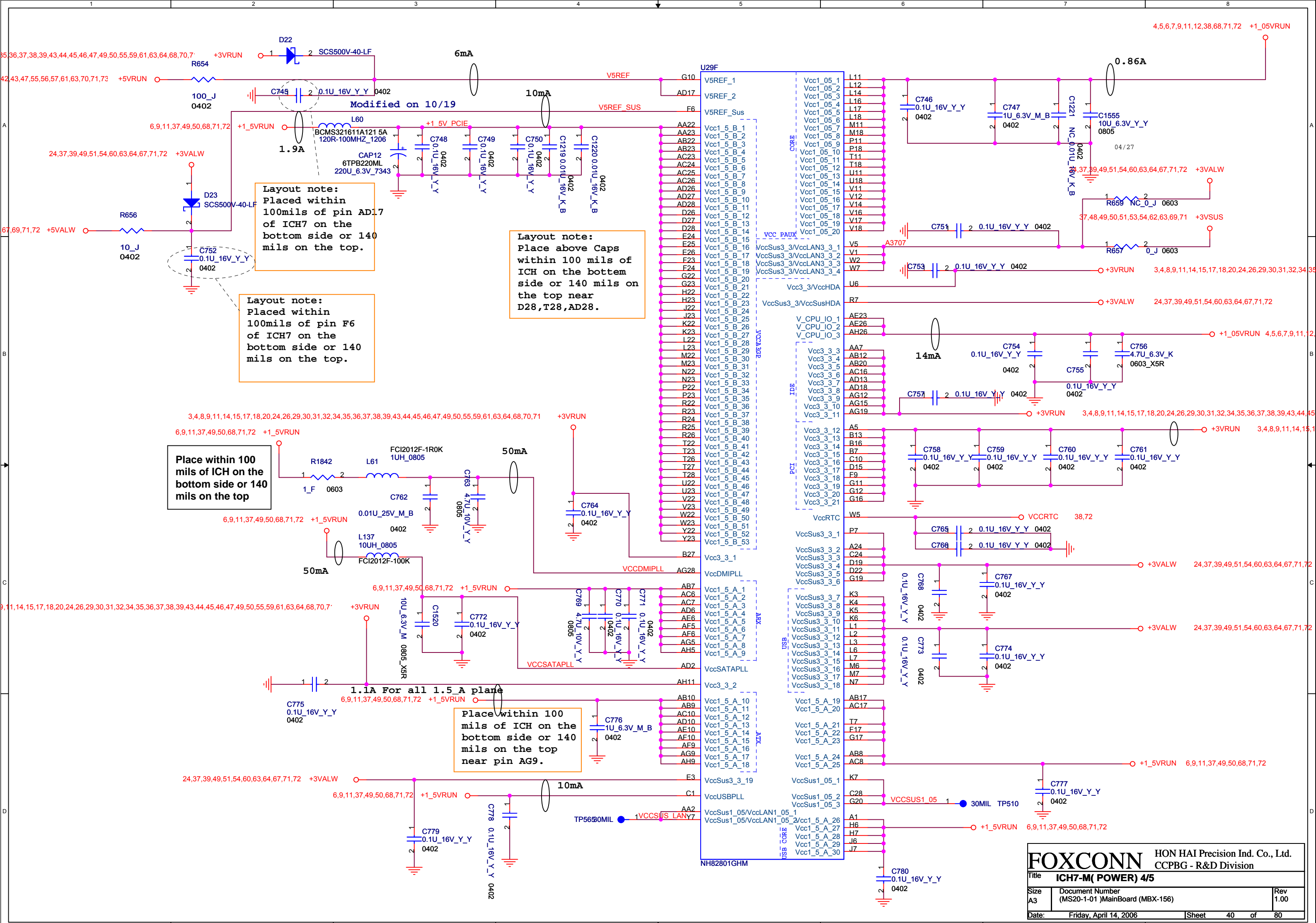


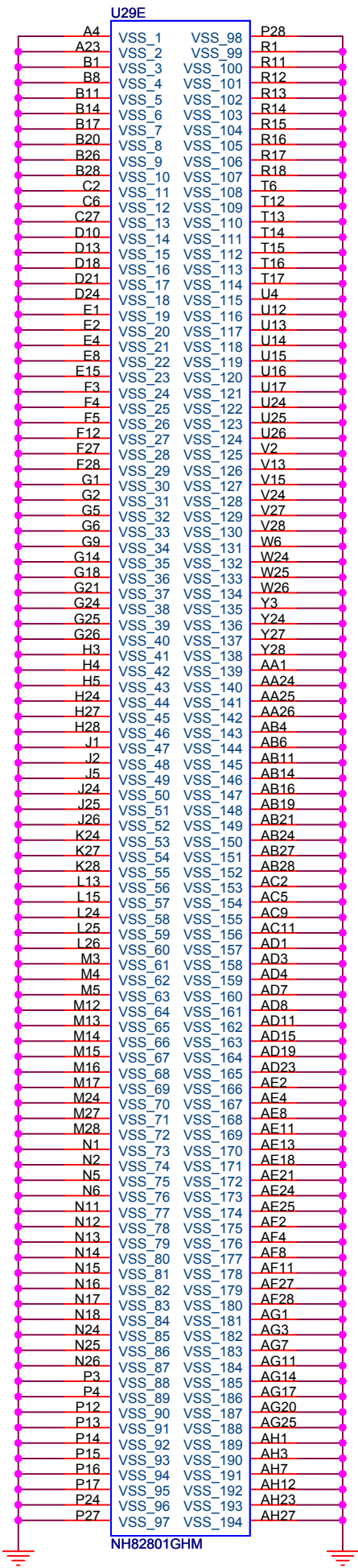
Place within 500 mils of ICH

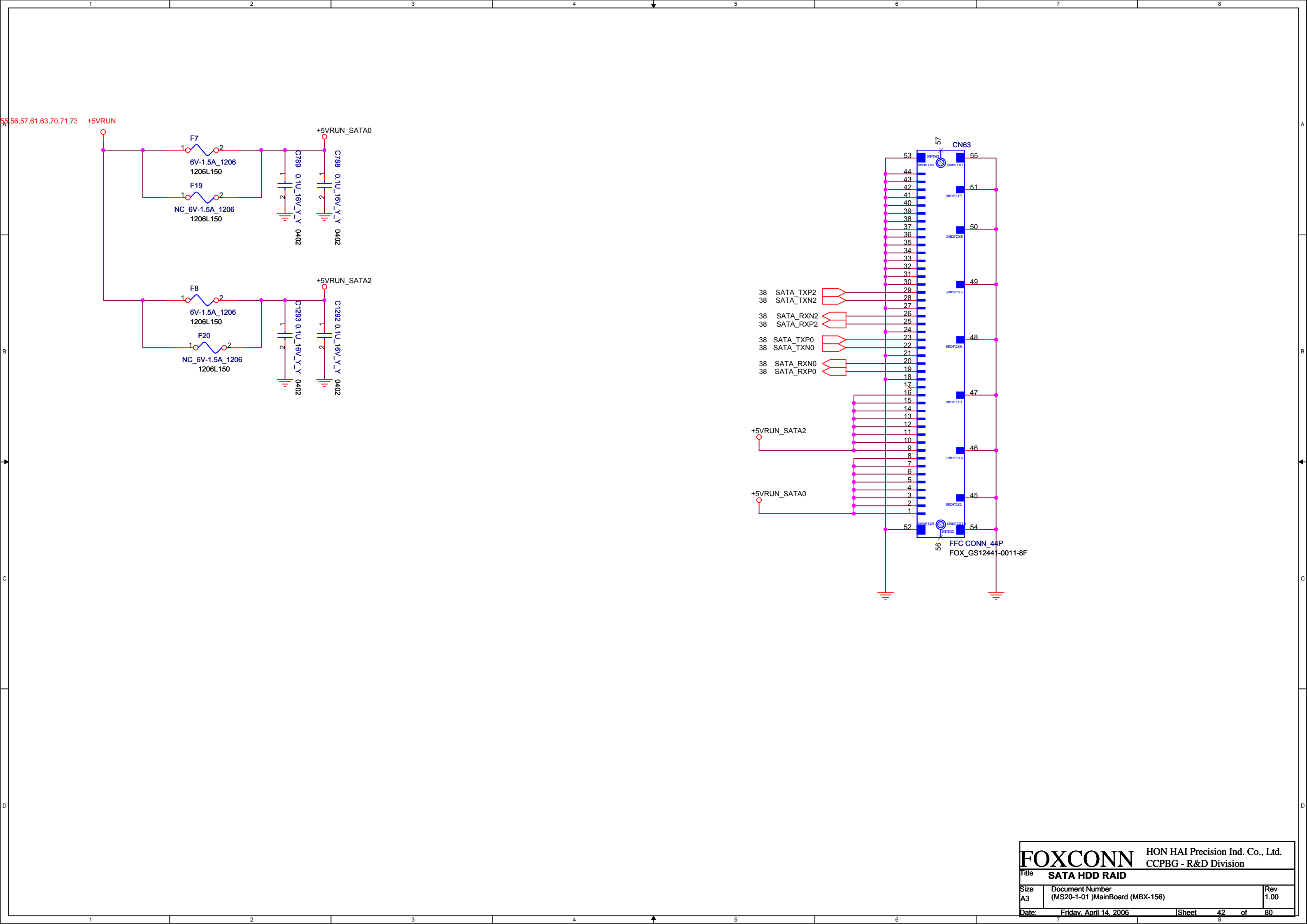
Place within 500 mils of ICH and don't routing next to high speed signals





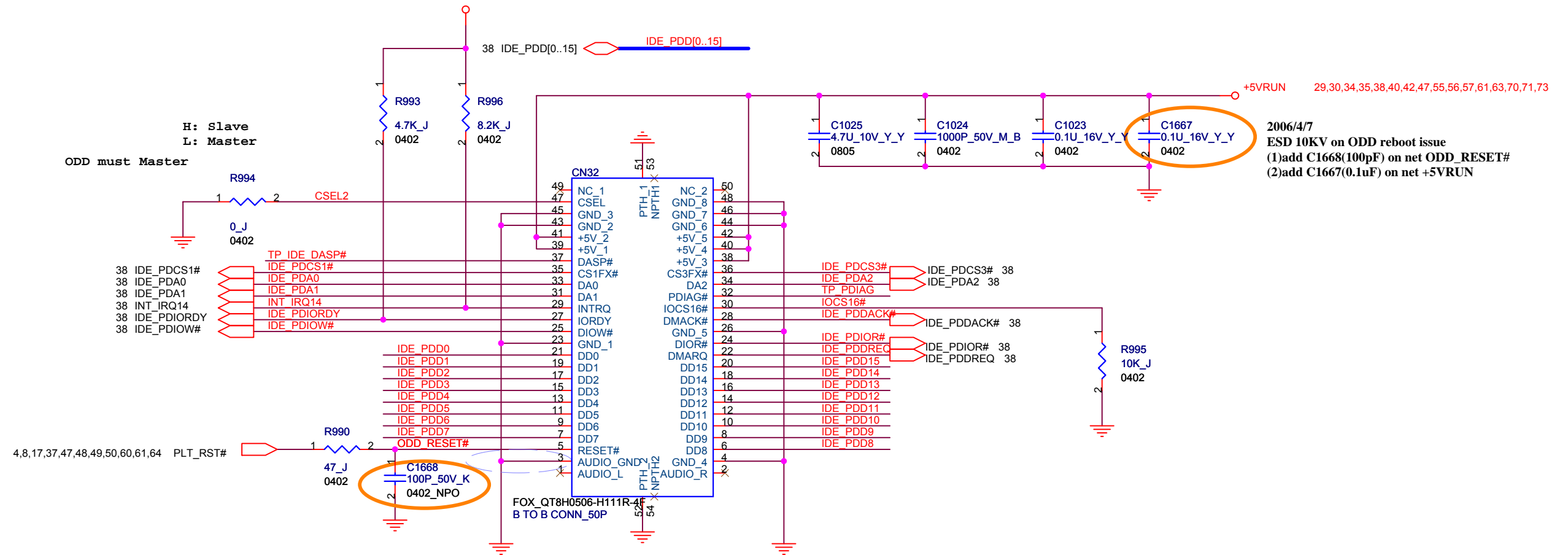






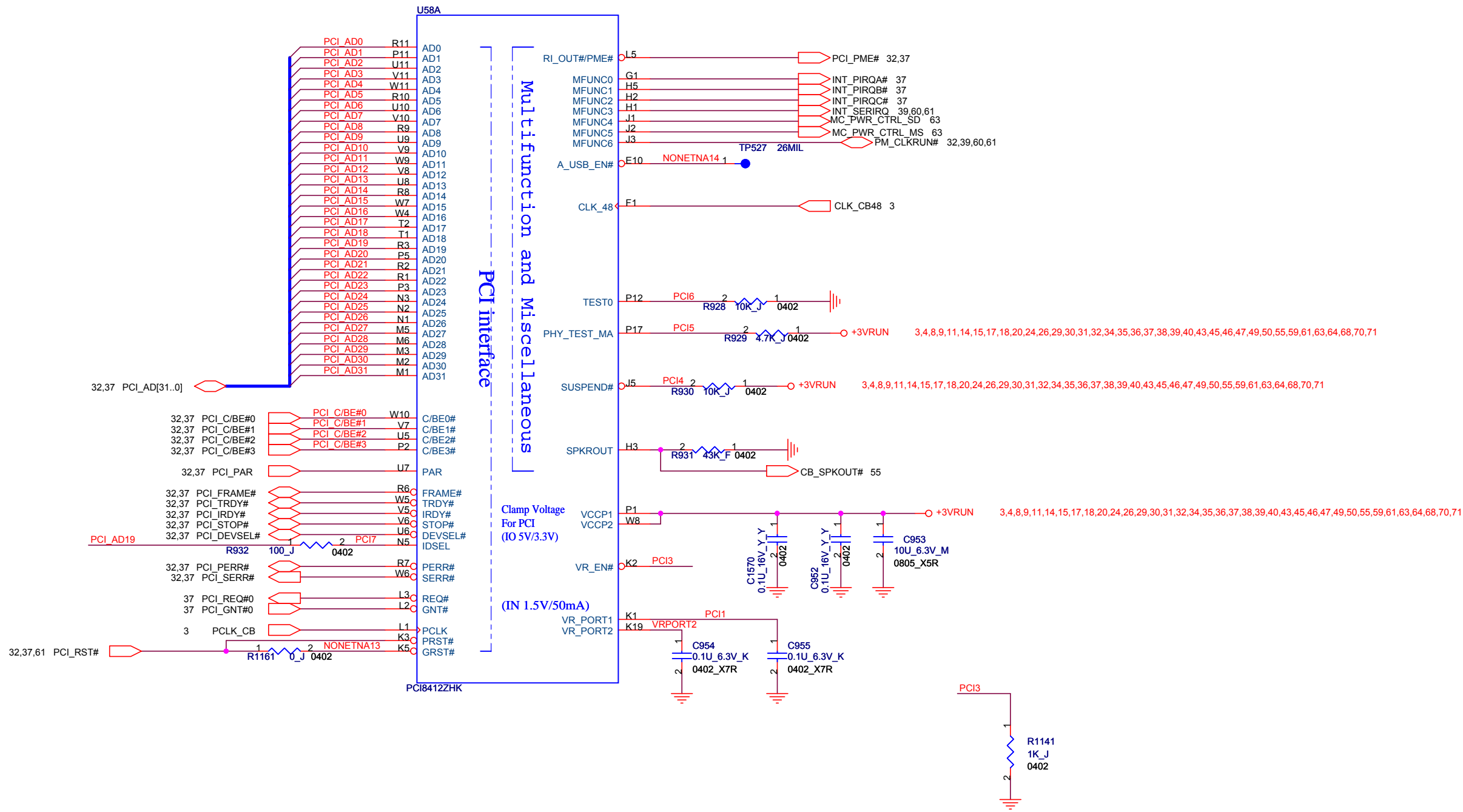
3,4,8,9,11,14,15,17,18,20,24,26,29,30,31,32,34,35,36,37,38,39,40,44,45,46,47,49,50,55,59,61,63,64,68,70,71

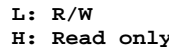
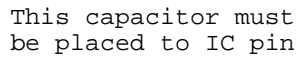
+3VRUN

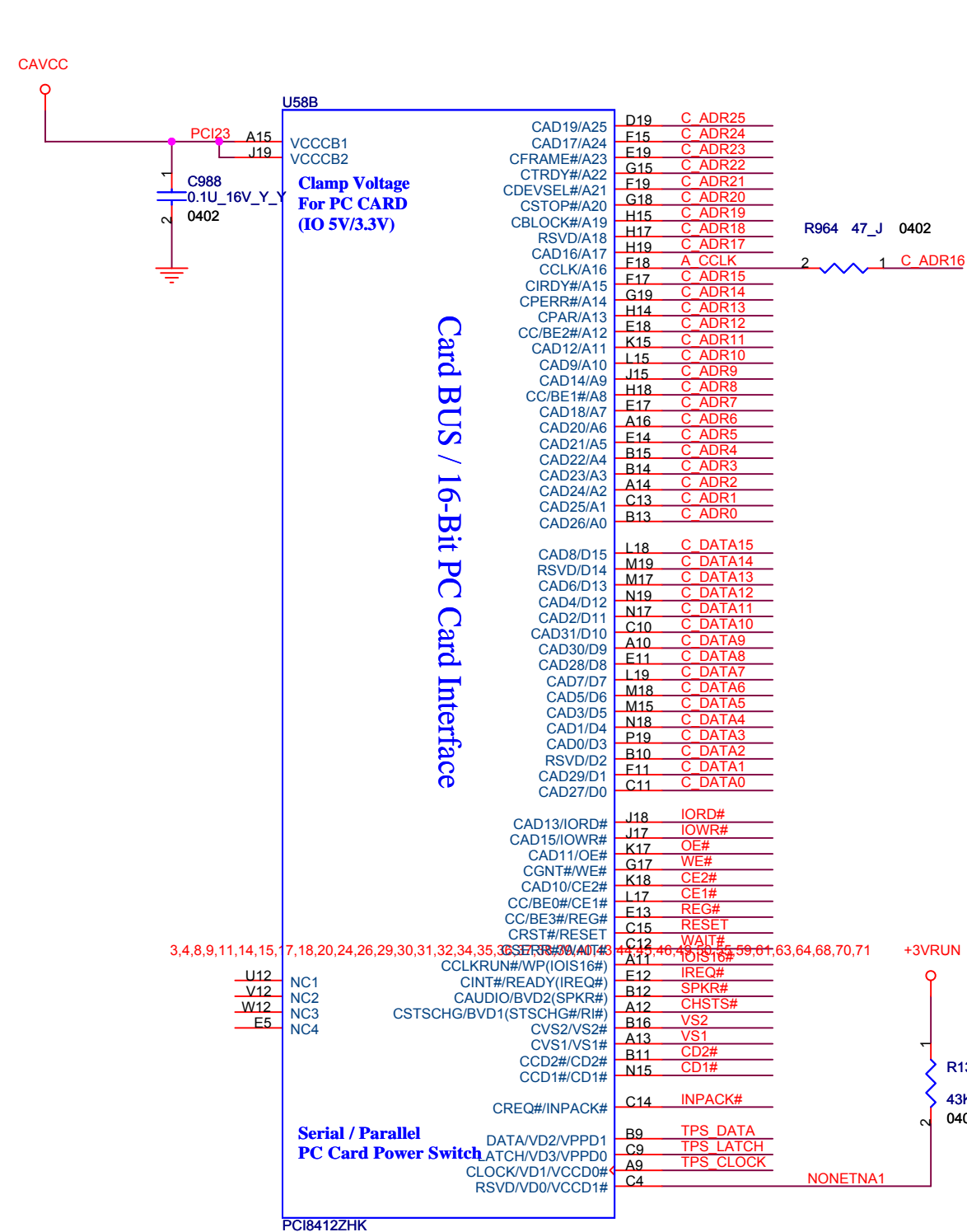


2005/4/17
Follow Adoi san suggest ODD: Master/HDD:Slave

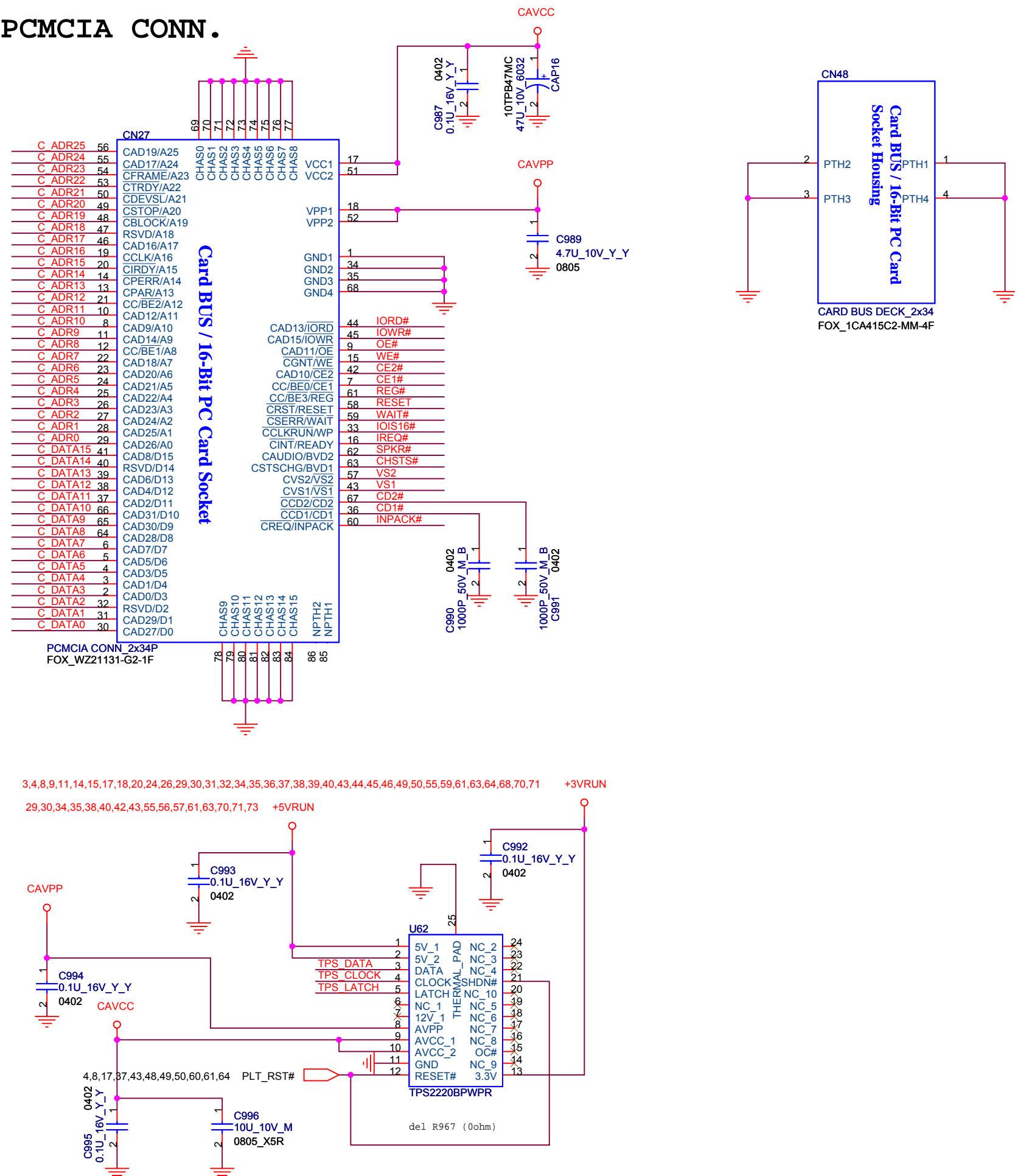
CD-ROM CONN

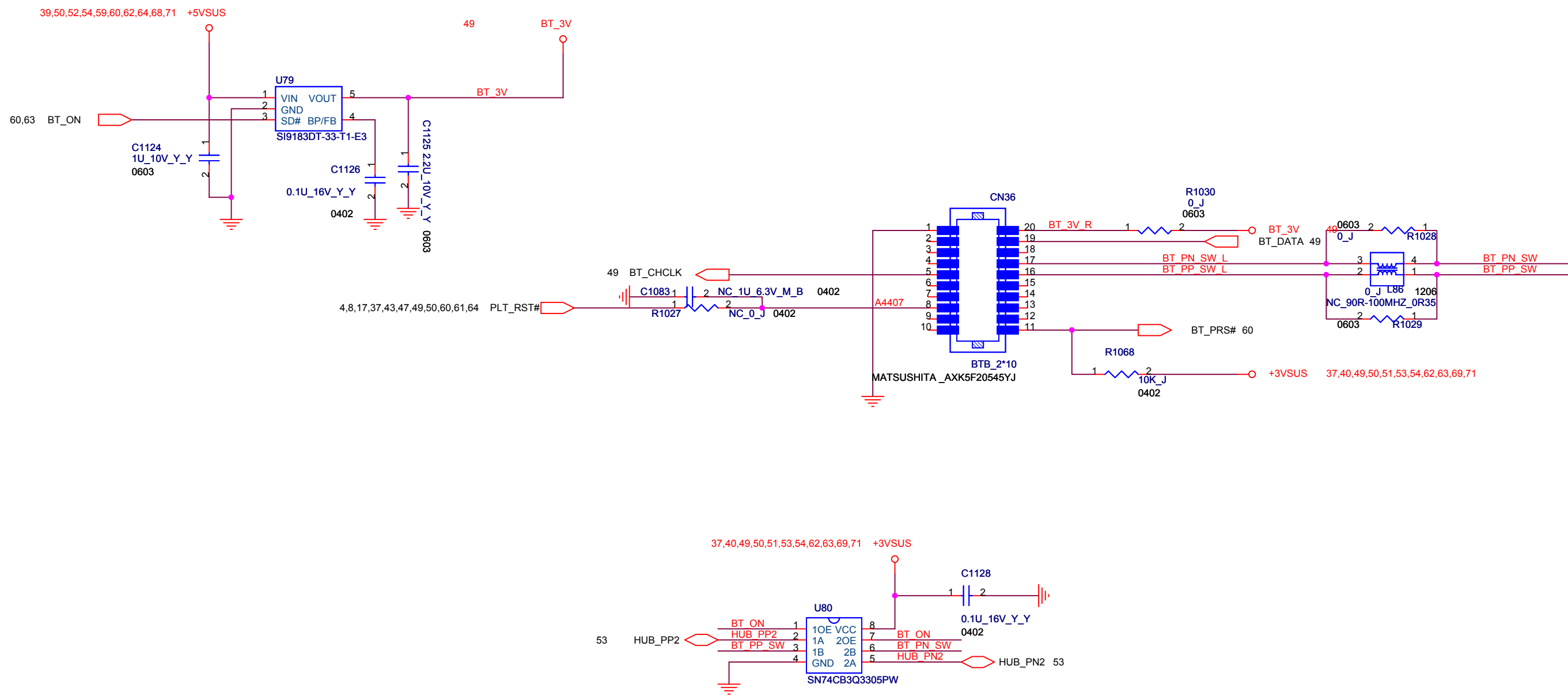


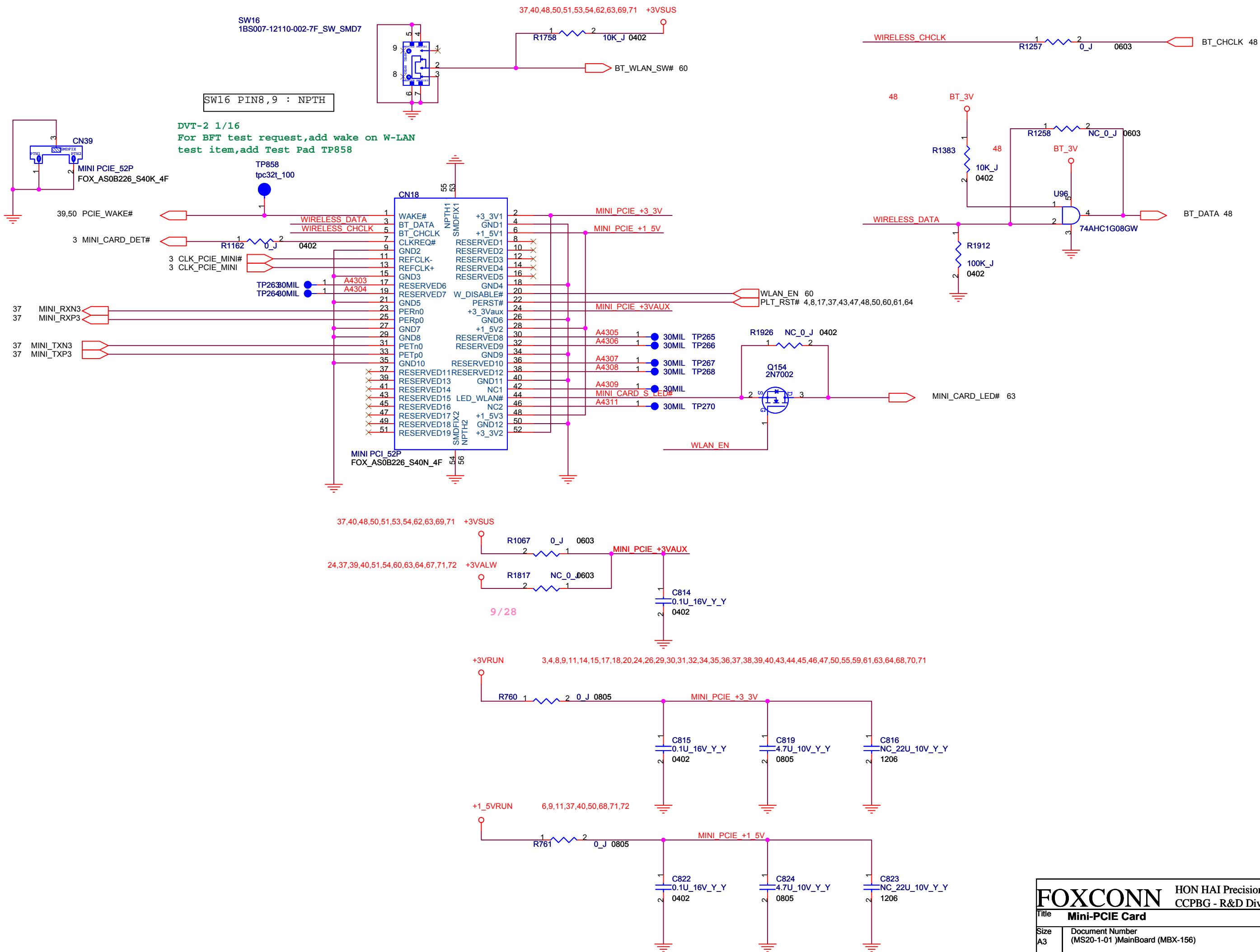


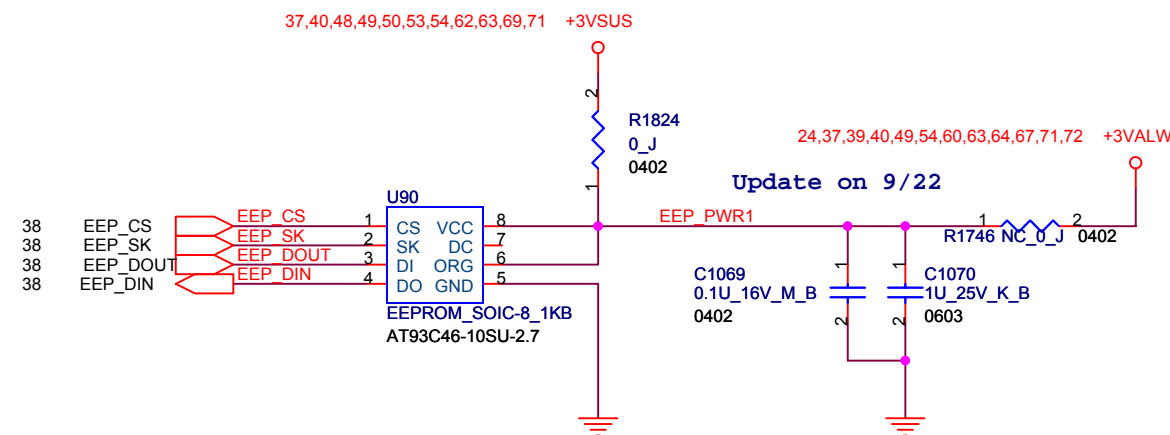
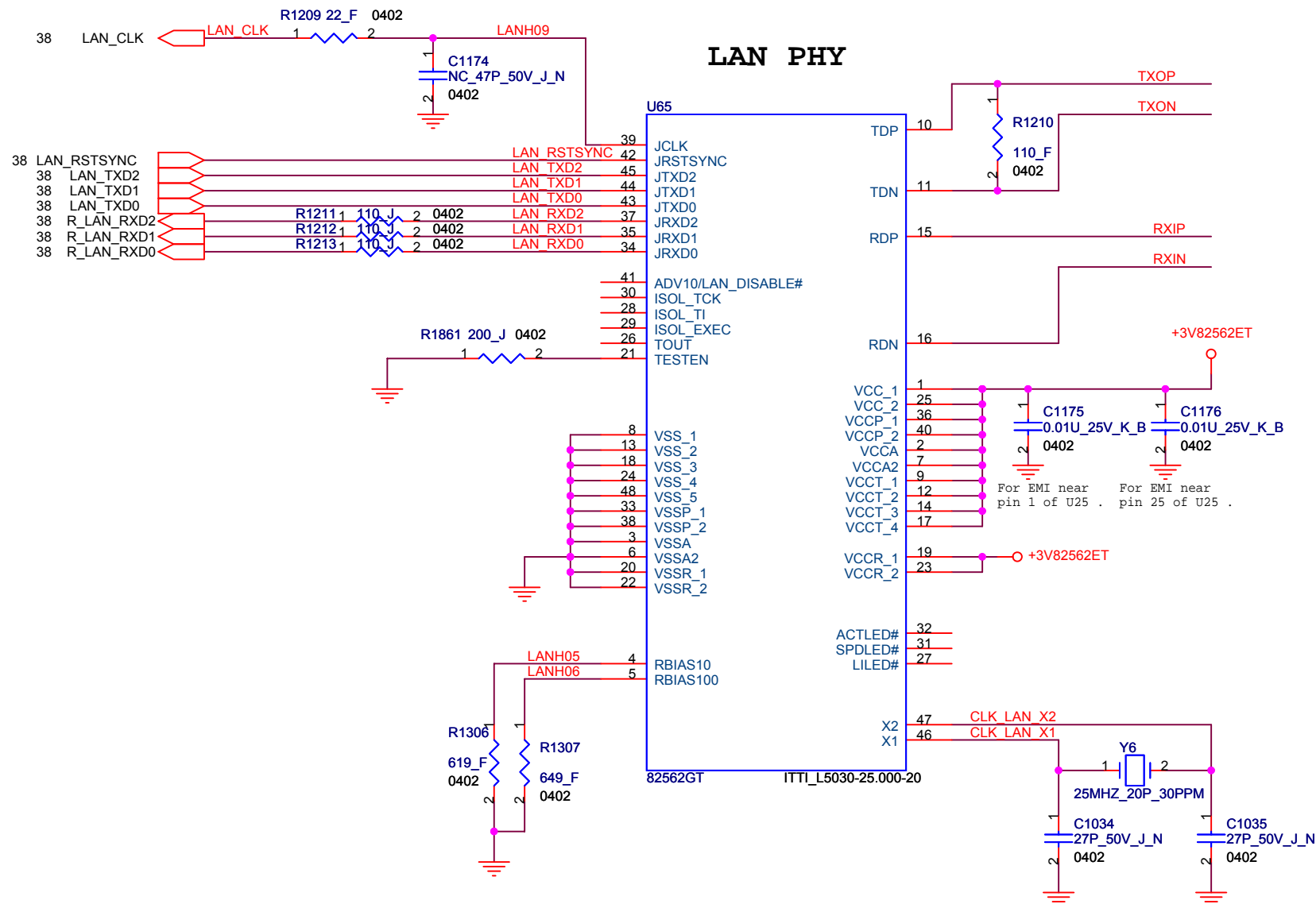
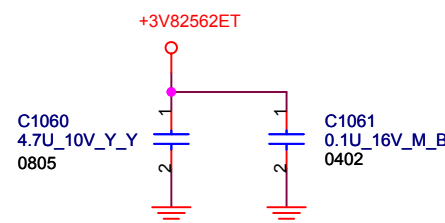
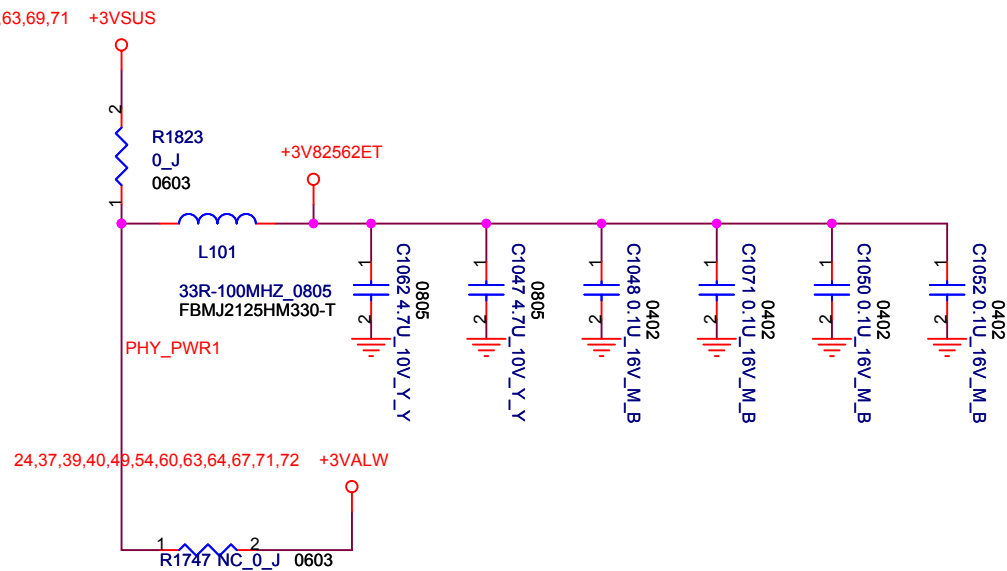
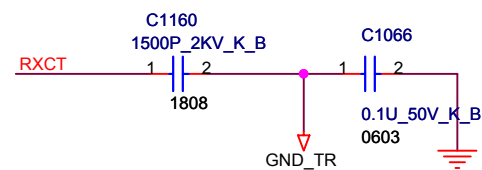
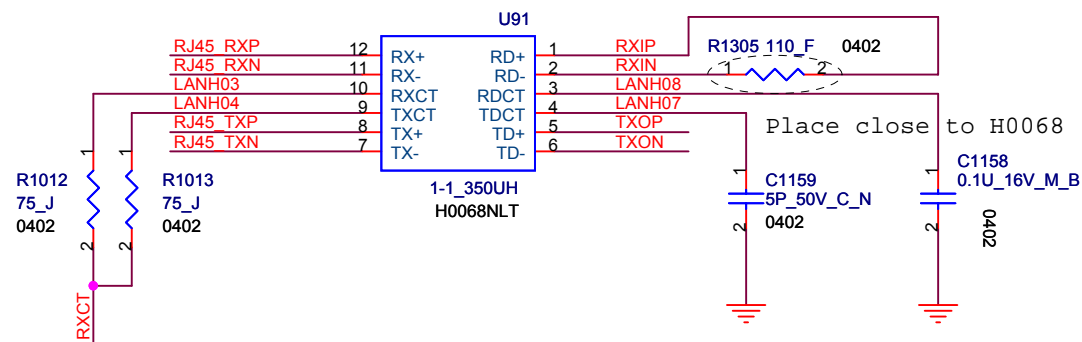
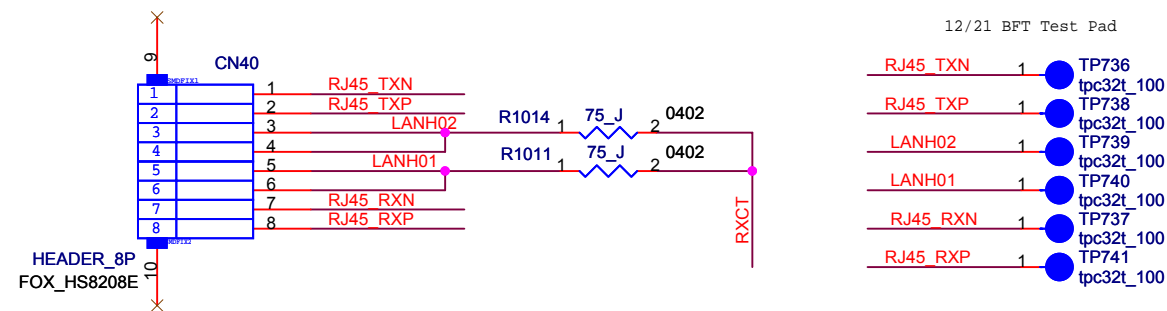


PCMCIA CONN.



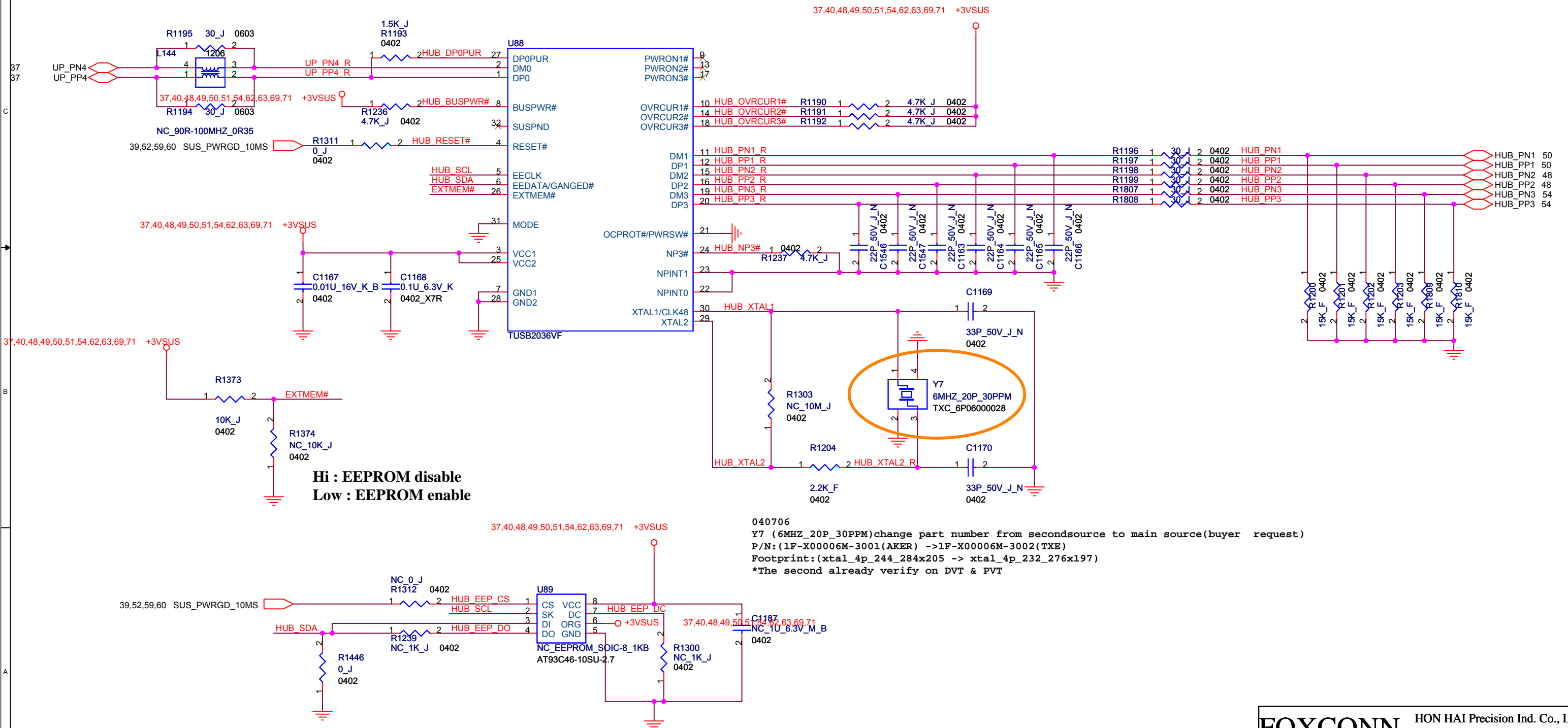






Default for S3 waking up event ,
 backup for S4 waking up event

**Application design in datasheet 27 ohm;
but 30ohm is also in range of USB Spec.**



040706
Y7 (6MHZ_20P_30PPM)change part number from secondsource to main source(buyer request)
P/N:(1F-X00006M-3001(AKER) ->1F-X00006M-3002(TXE)
Footprint:(xtal_4p_244_284x205 -> xtal_4p_232_276x197)
*The second already verify on DVT & PVT

030106: Change power
plan for leakage issue
of USB hub.

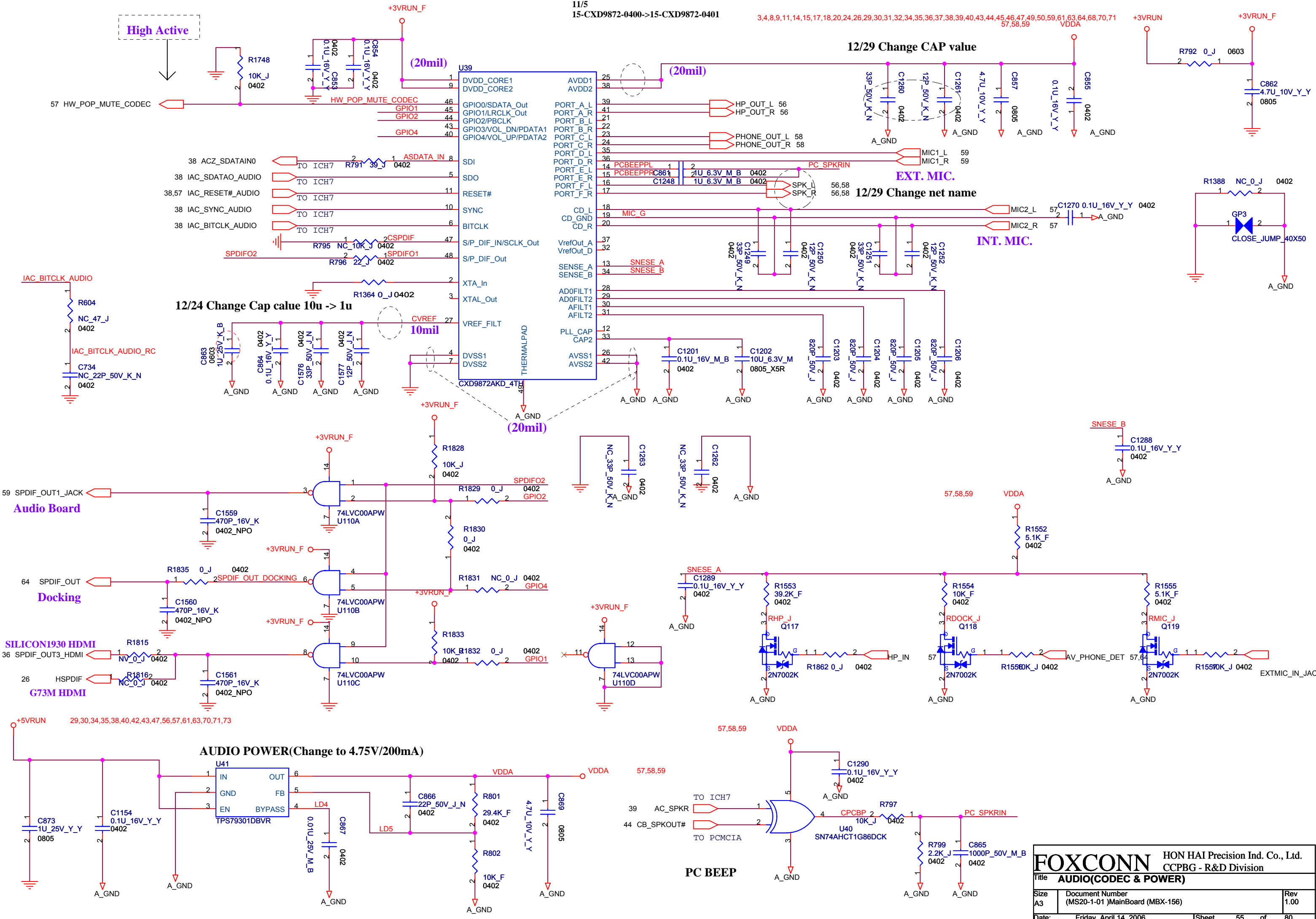
Change R1913 from 10K to 100K

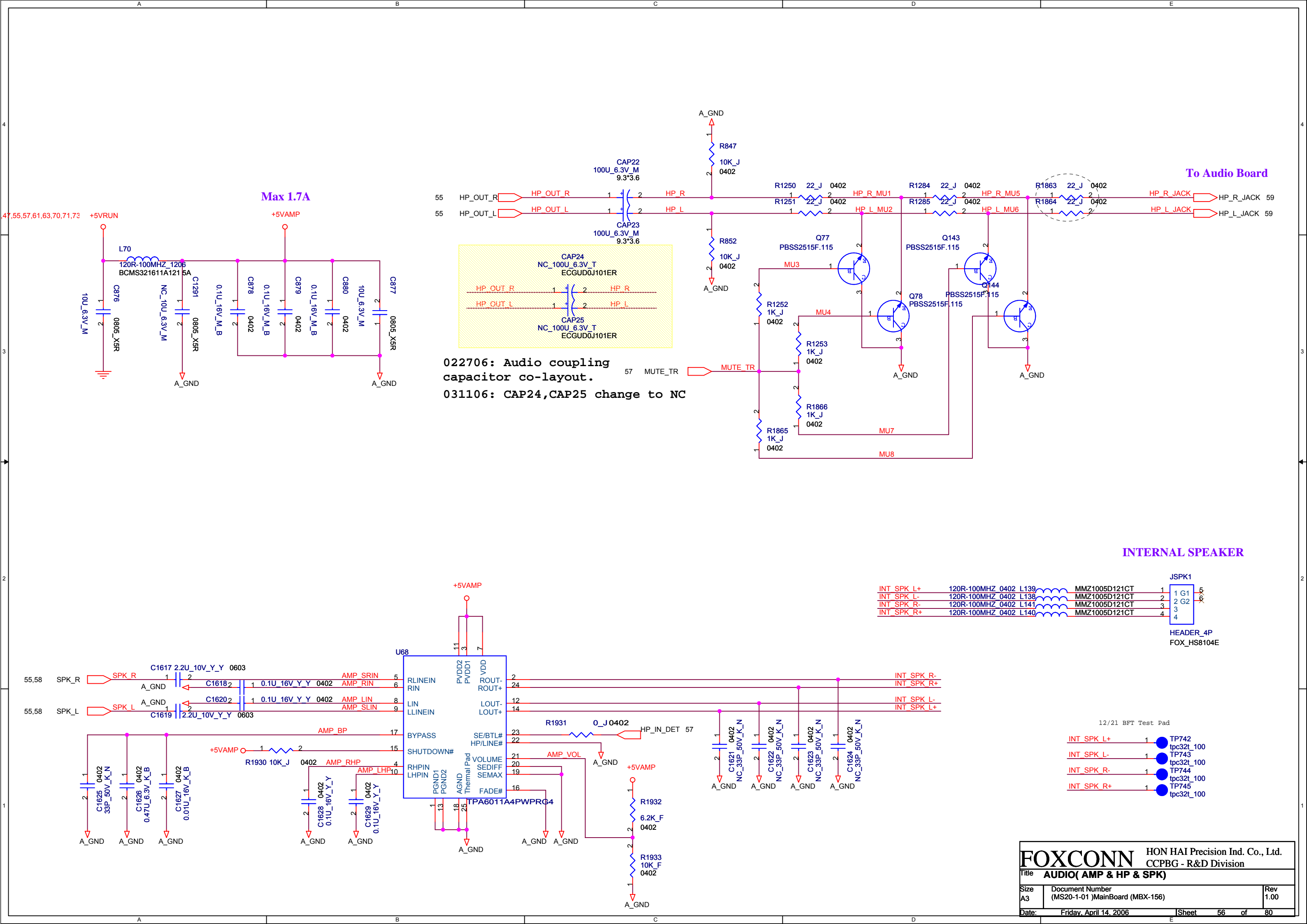
12/29 Add Pull High

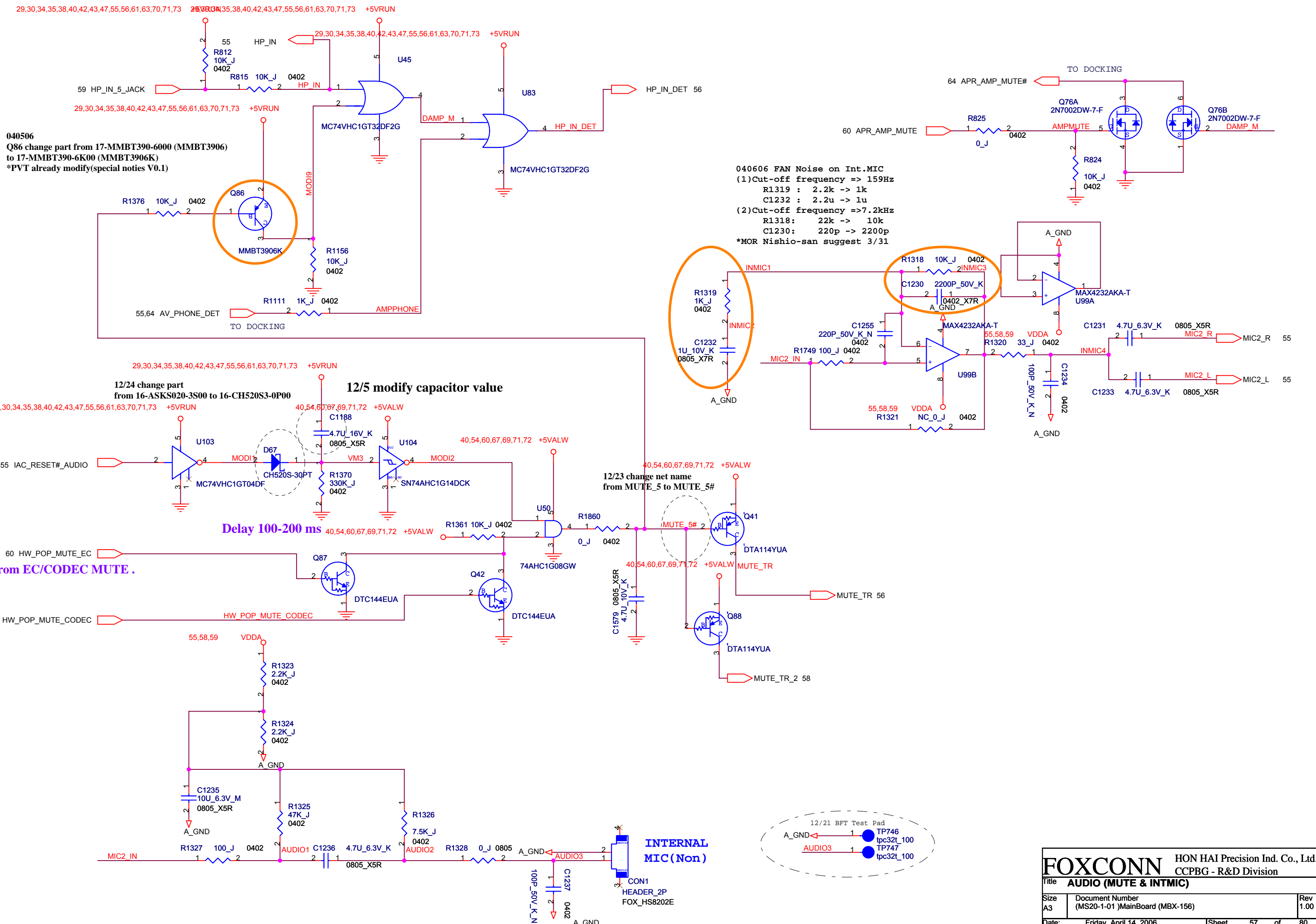
IR RECEIVER

040406:WA of InstantOn later(1)
IR receiver connentor side add N-MOS 2N7002(Q157)
for 3V->5V level shift
*PVT already modify(Rework Notice item#3)

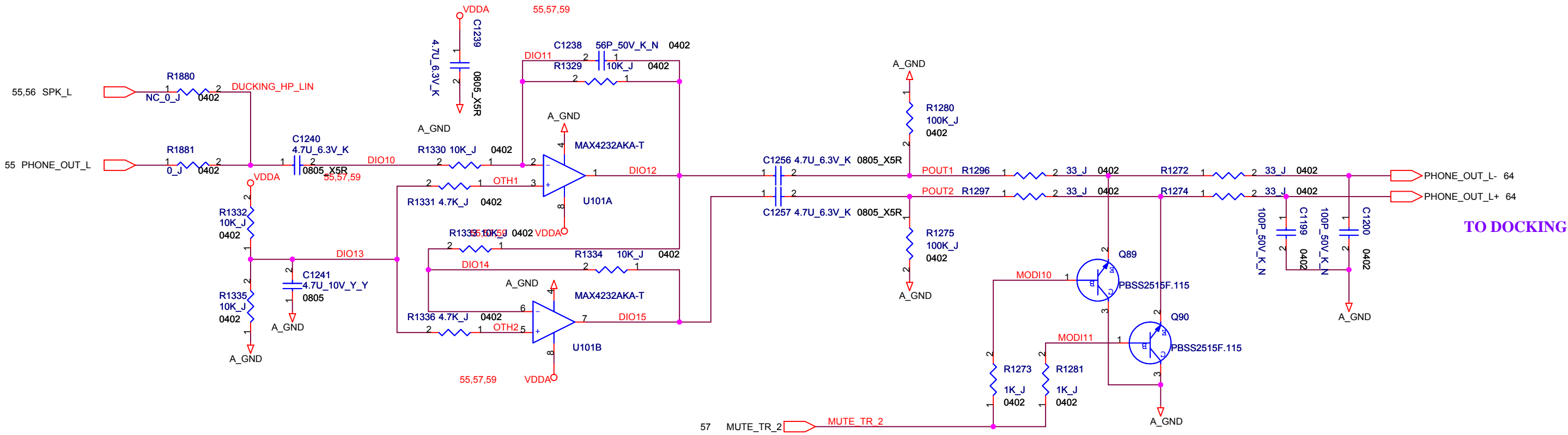
USB VCC F	1	TP847
USB PP3 F	1	tpc32t_100
USB PN3 F	1	TP848
	1	tpc32t_100
	1	TP849
	1	tpc32t_100
	1	TP850
	1	tpc32t_100
CIR_ALPS_3VPU	1	TP851
	1	tpc32t_100
SW_CIR00	1	TP852
	1	tpc32t_100
SW_CIR01	1	TP853
	1	tpc32t_100
SW_CIR02	1	TP854
	1	tpc32t_100
PWR_CIR#	1	TP855
	1	tpc32t_100
CIR_ALPS_SPWR	1	TP856
	1	tpc32t_100



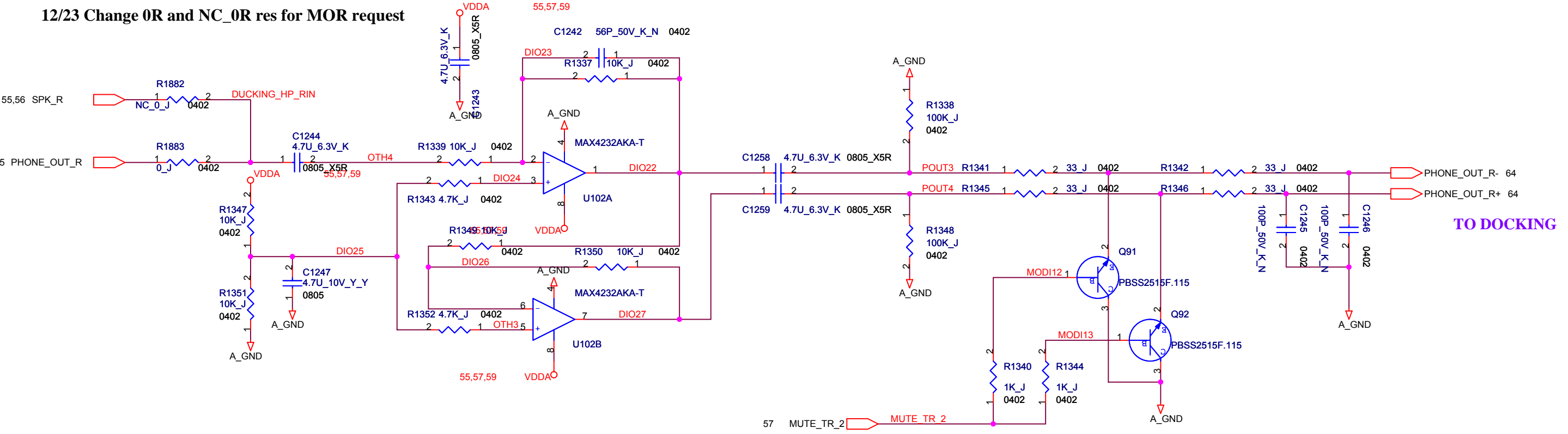


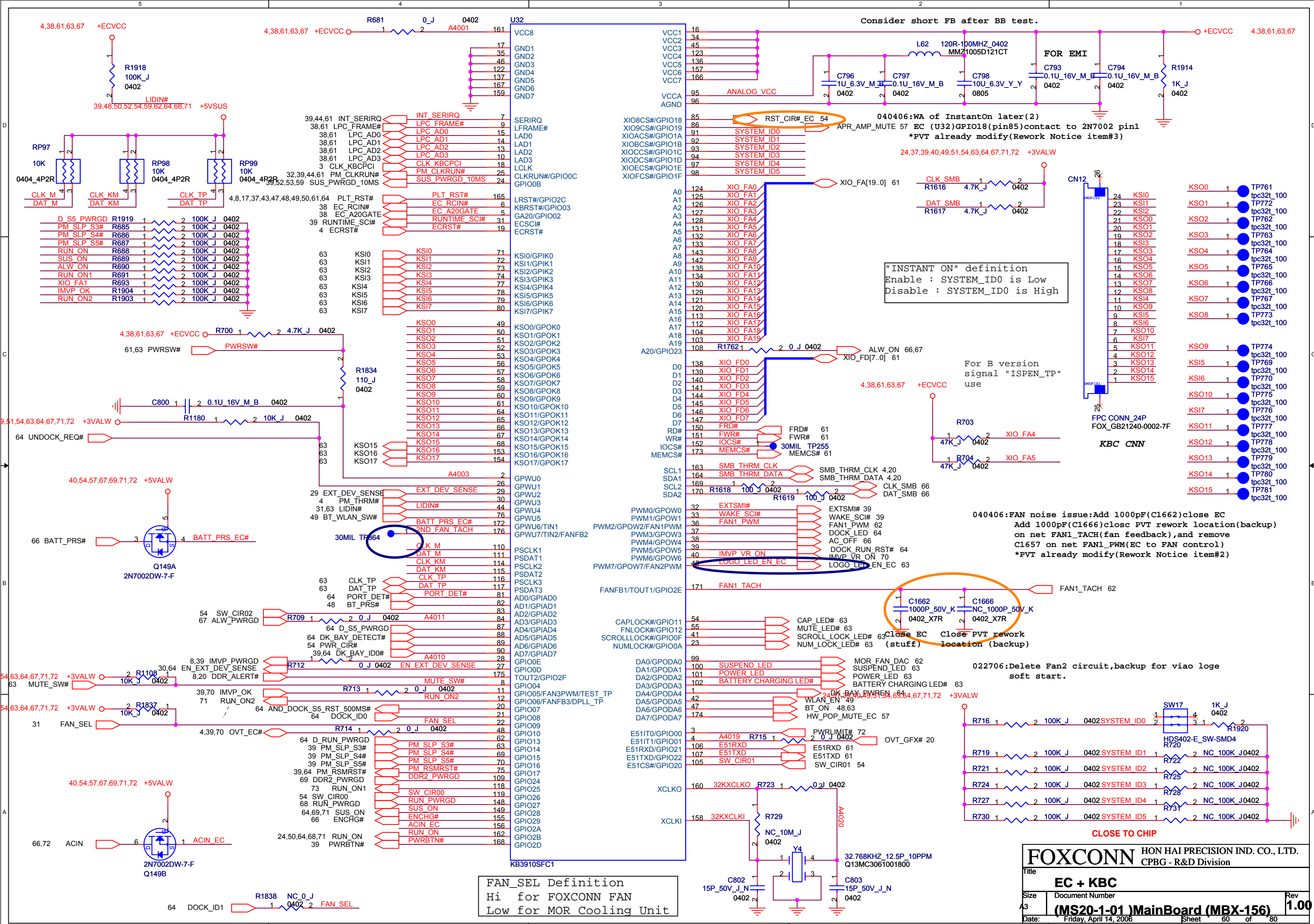


PHONE OUT



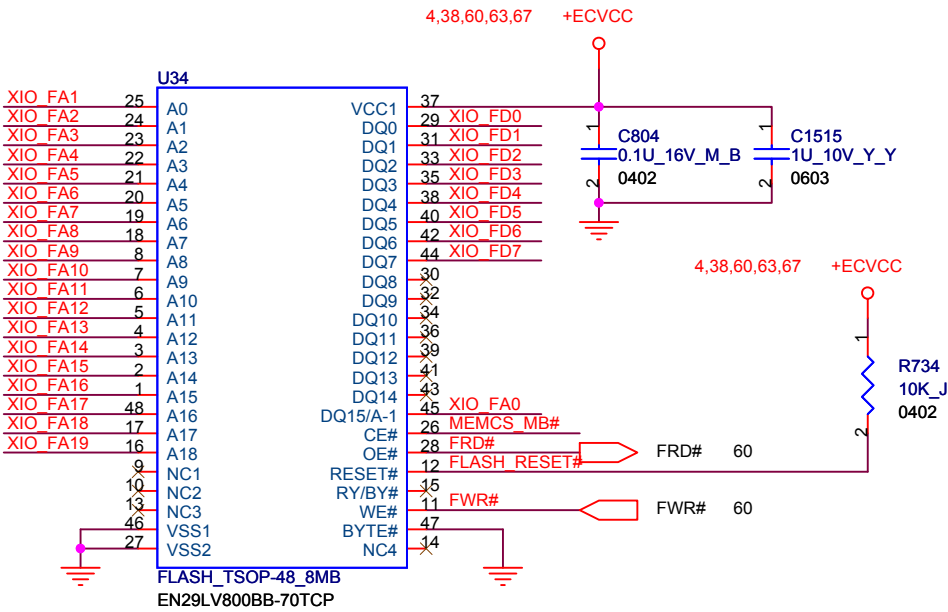
12/23 Change 0R and NC_0R res for MOR request



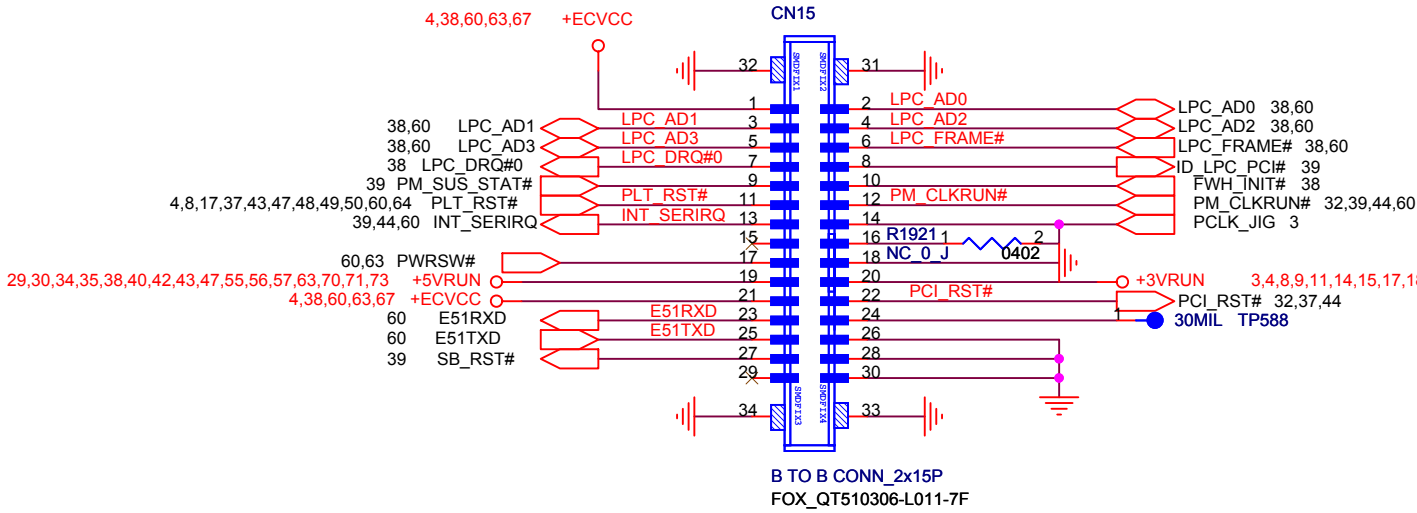


60 XIO_FA[19..0]

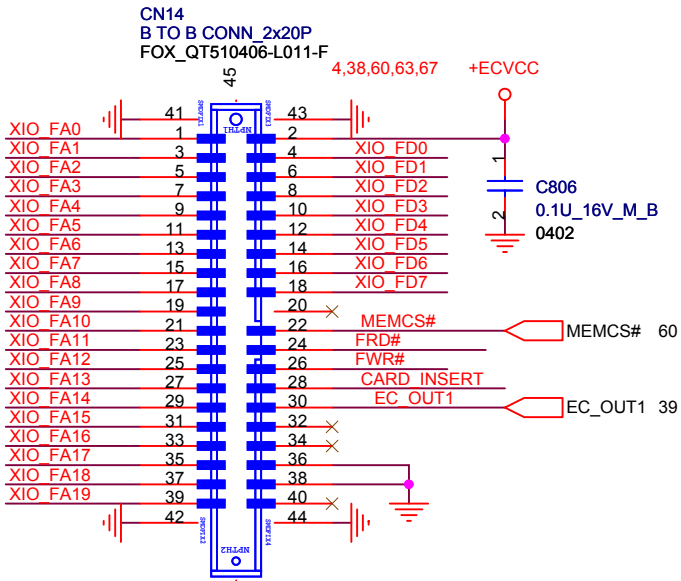
60 XIO_FD[7..0]



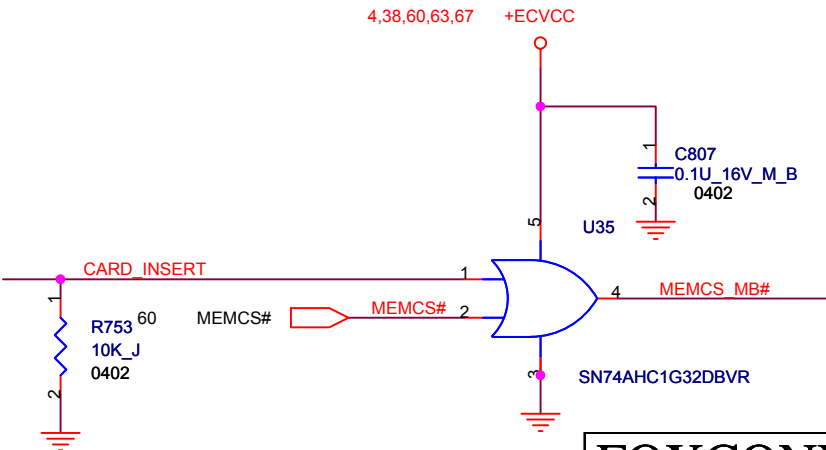
FLASH BIOS



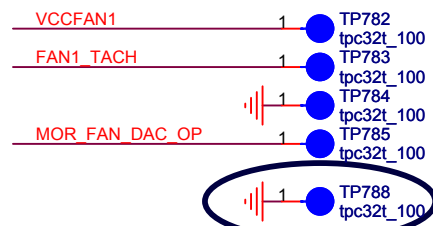
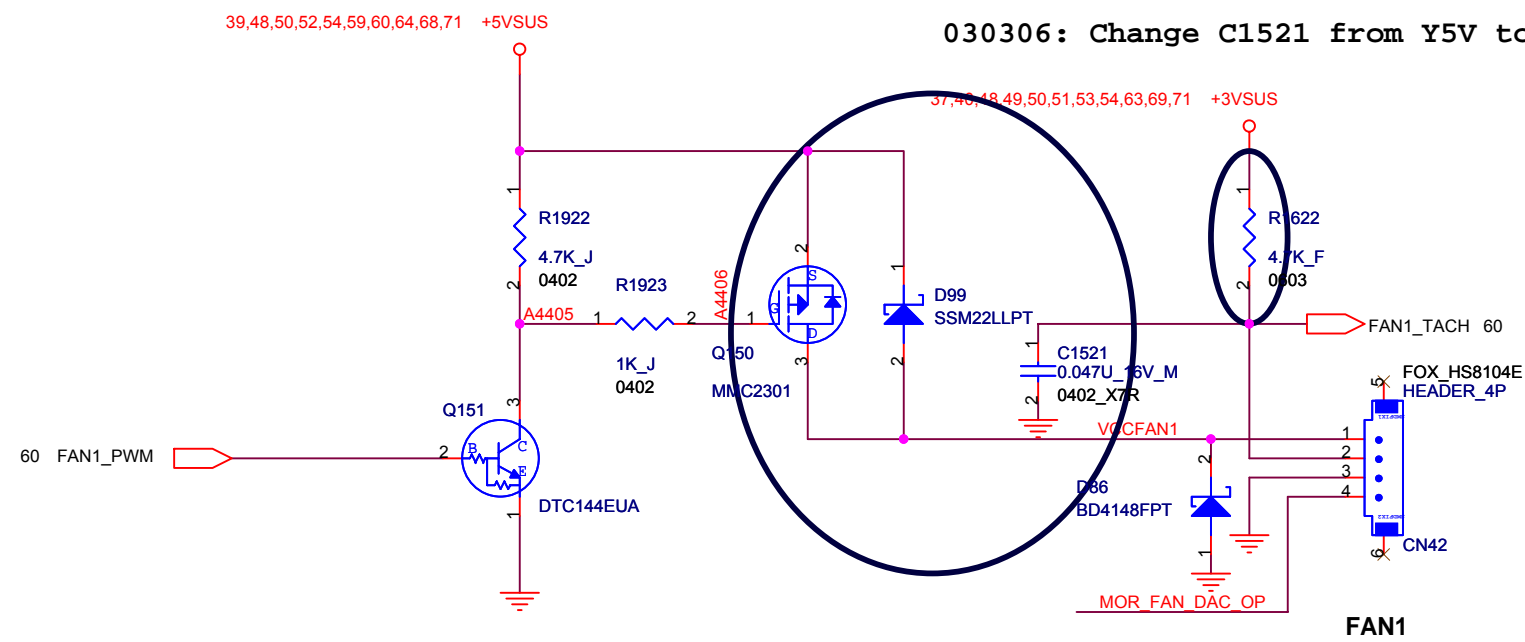
JIG-120



X-BUS



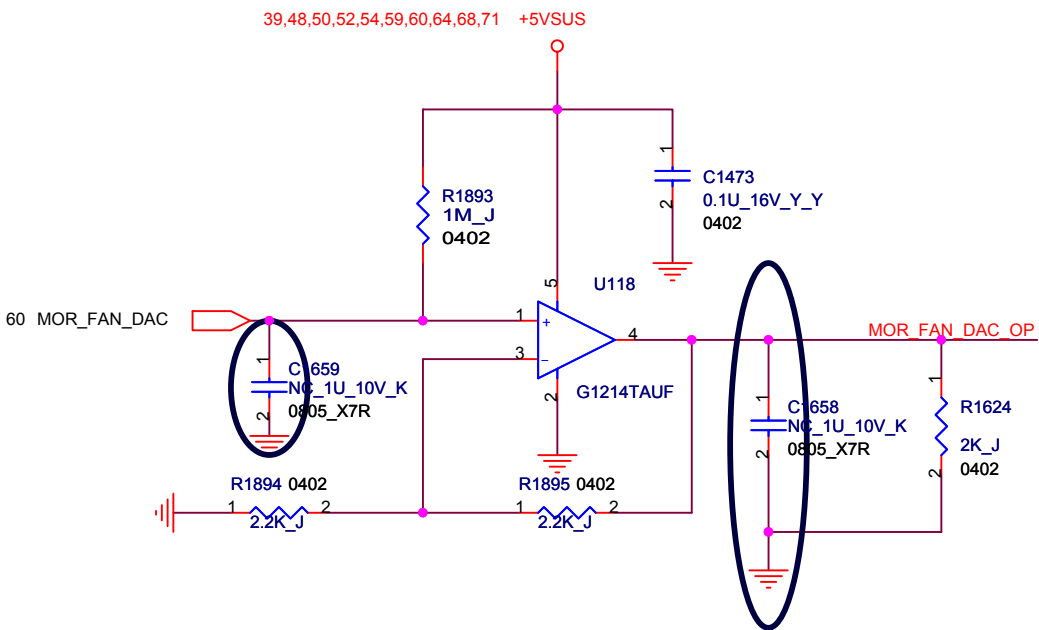
022706: Add doide for inverse current and change pull-high resistor from 10K to 4.7K.



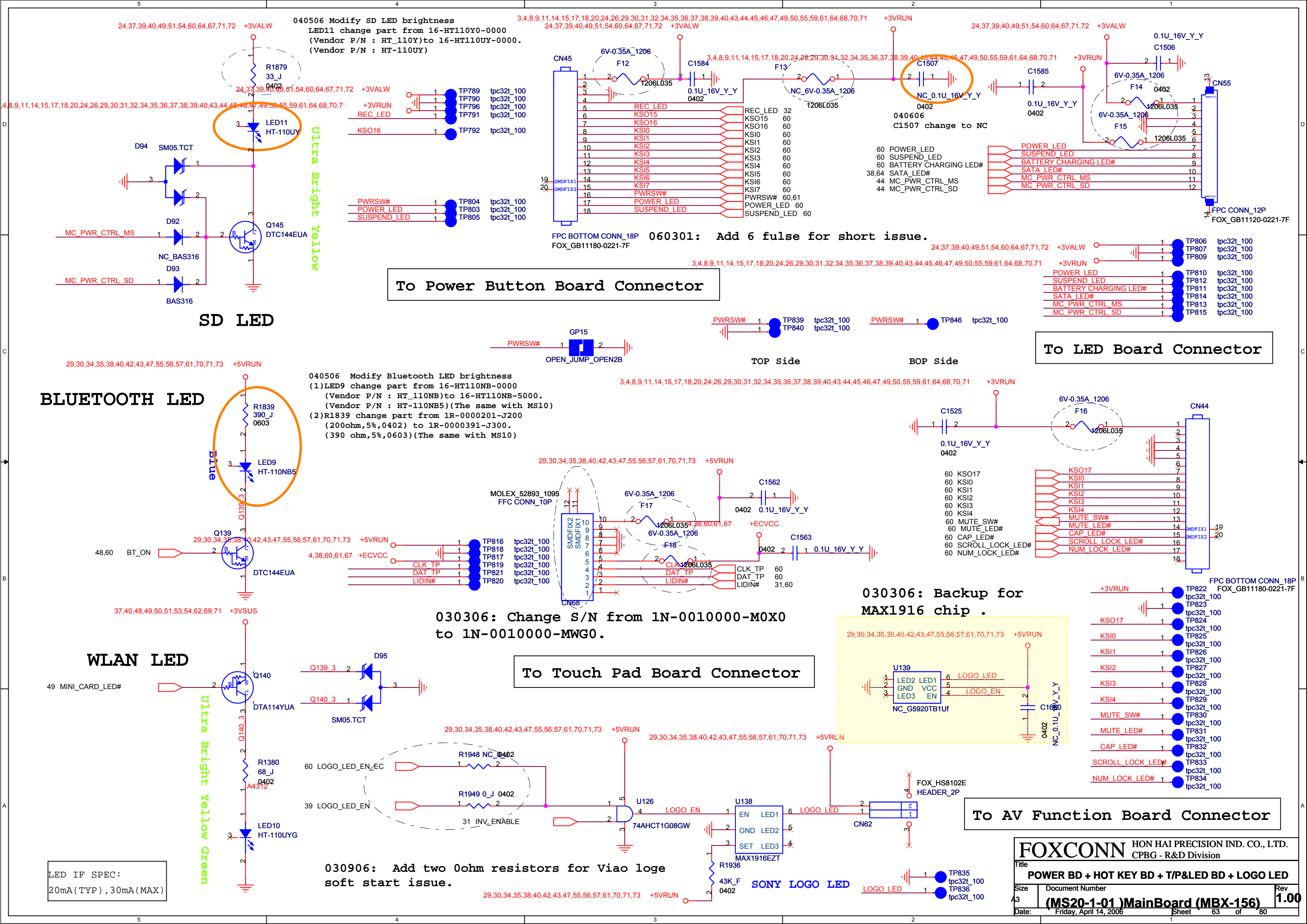
030506: Backup Test Pad.

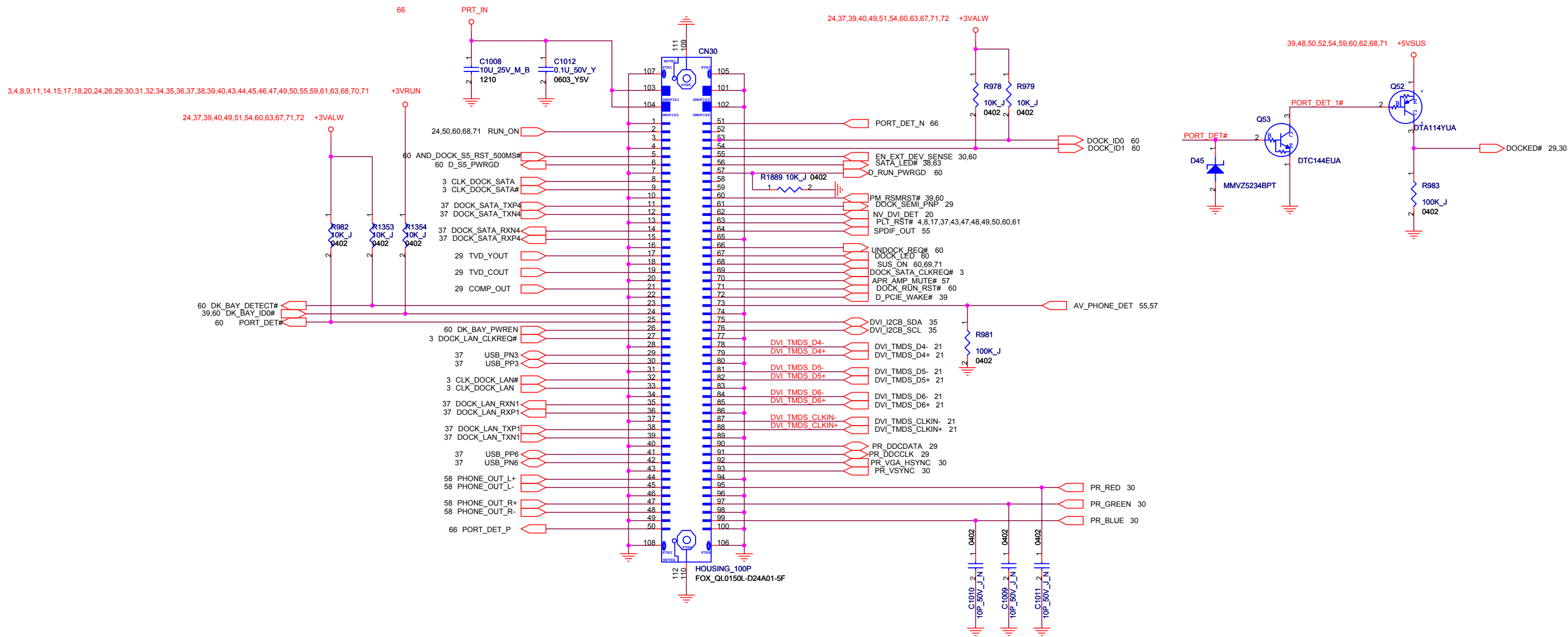
FAN(FAN1+MOR FAN)

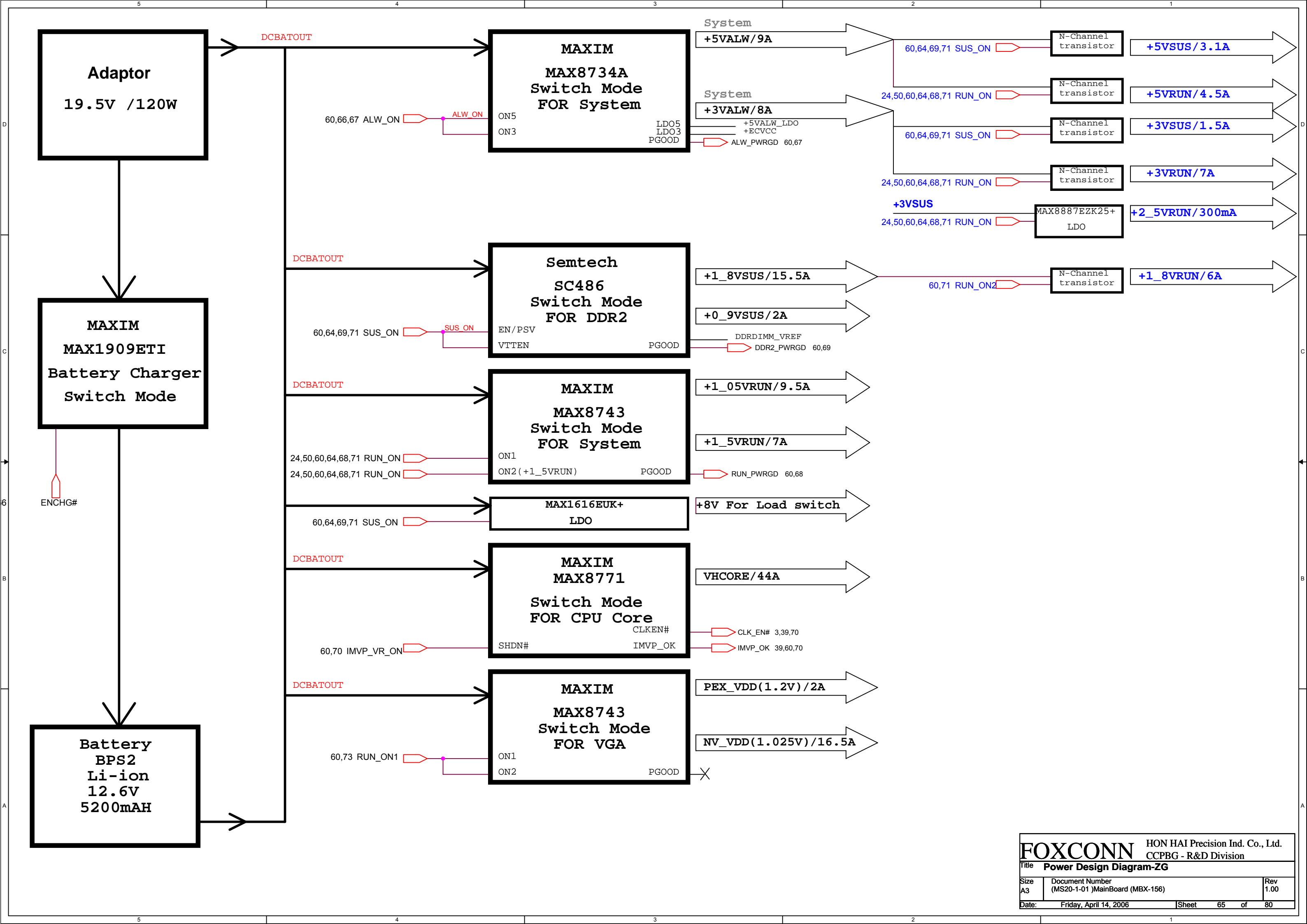
030306: Delet FAN2 circuit.

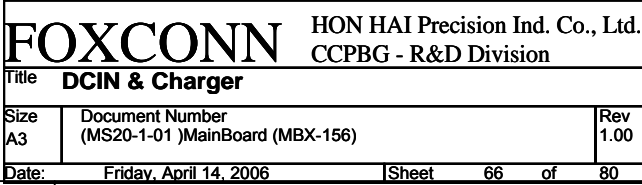


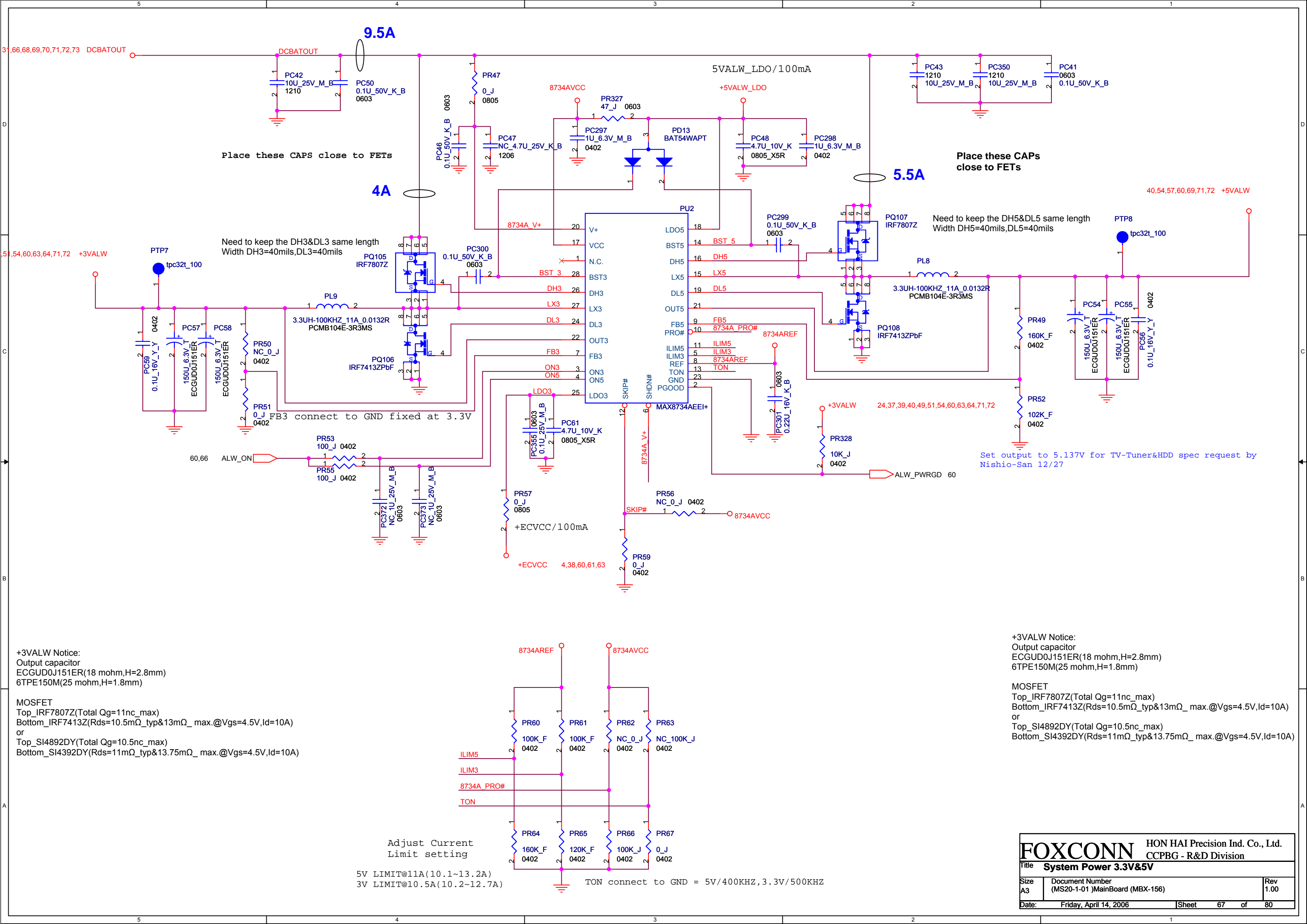
022706: Add capacitor for cooling unit.
031106: C1658 change to NC

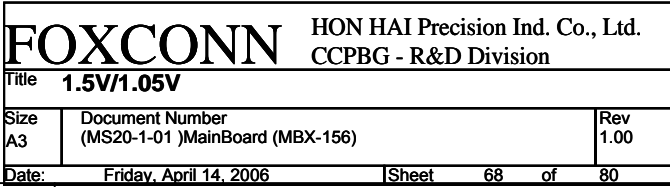


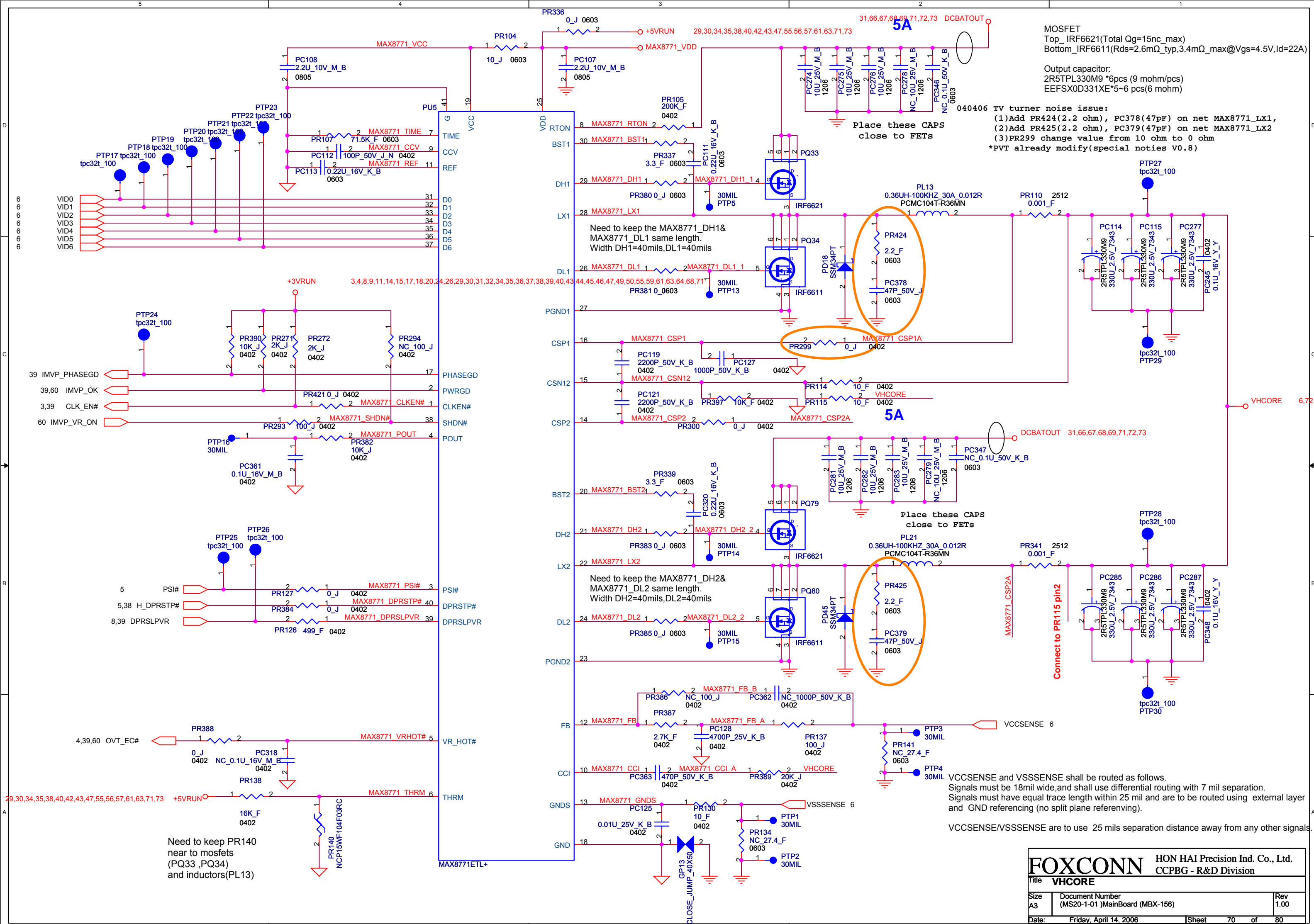


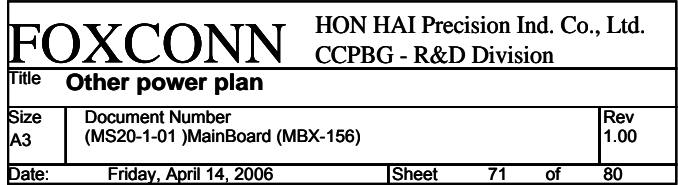


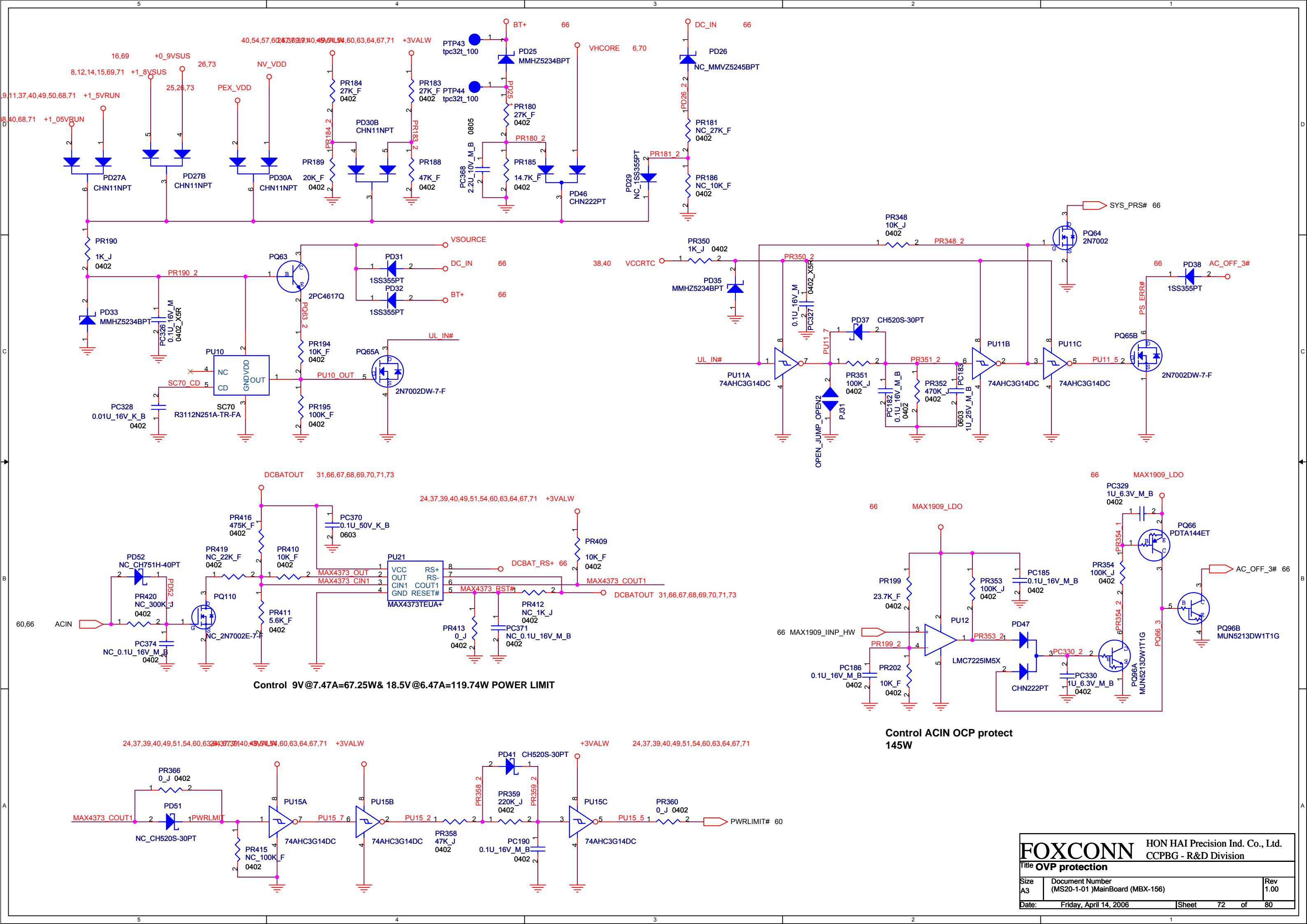










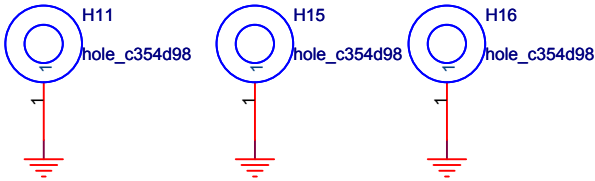


Control 9V@7.47A=67.25W& 18.5V@6.47A=119.74W POWER LIMIT

Control ACIN OCP protect
145W

HOLE

Type 1



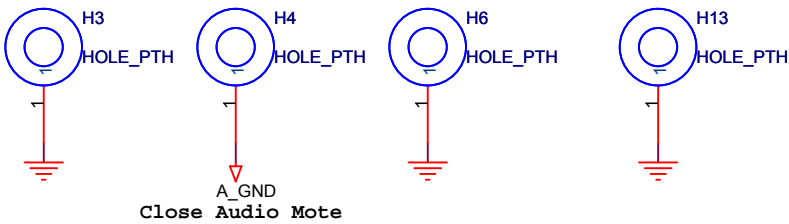
Type 2

10/24
Remove Screw Hole H2
P/N 1X-HOLE000-0108
beacuse the Hole overlay
with CN32 and layout will
modify component screw shipe

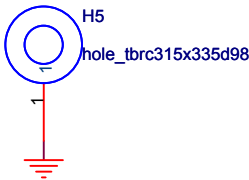
Type 3

10/24
Remove Screw Hole H1
P/N 1X-HOLE000-0110
beacuse the Hole overlay
with CN32 and layout will
modify component screw shipe

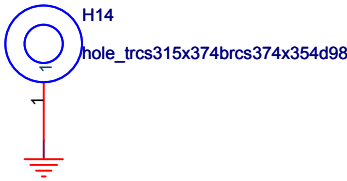
Type 4



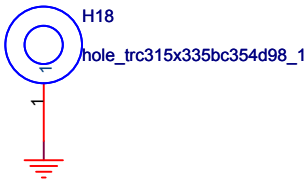
Type 5



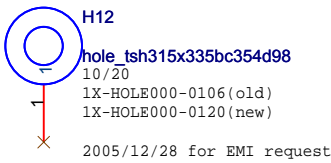
Type 6



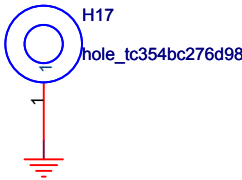
Type 7



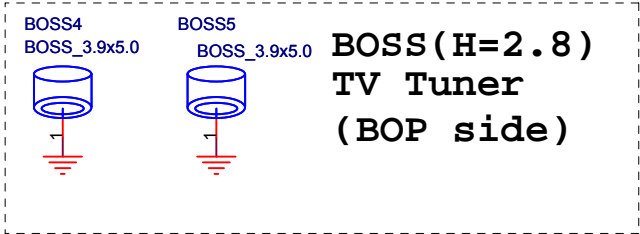
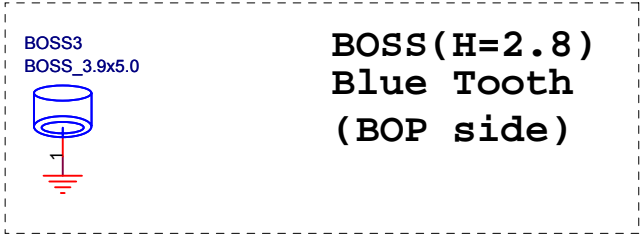
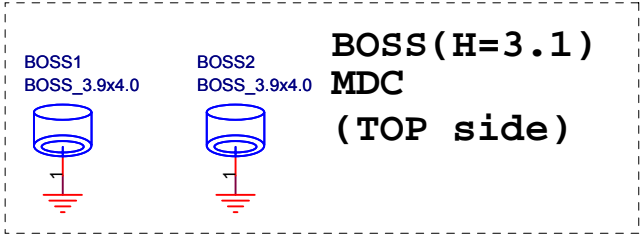
Type 8



Type 9



Type CPU



Type NPTH Guide (spherical)HOLD



Type NPTH Guide (oval-shaped)HOLD



(2005/09/19)

- 1.Update the NB and CPU circuit base on intel new design guide revision 1.5
- 2.Changed the wake event from S3 to S4 for lan .
- 3.Modified the MS current resistor from 1K to 1.5K to meet customer specification.
- 4.Express card power plane changed.
- 5.SB some power changed .
- 6.Modify HDMI circuit
- 7.Back Part value "NV"
- 8.Replease LVDS of 945GM interface

(2005/09/21)

- 1.Oide power plane change from 5VSUS to 5VRUN on page 48.
- 2.C1131 was connected to net "+1_5V_PCIE_OUT" on page 48.
- 3.Change R1672~R1675 from stuff to no sutff on page 34.
- 4.Add one series 0ohm resistor to net "1930_ACZ_SDIN2" on page 34.
- 5.Add pull-up resistor to LDDC_CLK/DATA and L_CLKCTLA/CLKCTLB according to intel design guide on page 9.
- 6.ODD/SATA HDD change power plan from SUS to RUN
- 7.CN19/CN47/CN26 updata CIS Library
- 8.CN26 MDC modem Pin 2-Pin 6 short
- 9.CN12 KB connentor change type updata CIS library

(2005/09/22)

- 1.CN48 change from P/N:1N-1080000-0000 to P/N:1N-1068000-0000
- 2.page 72 add battery in current limit protection
- 3.page 66 modified battery input circuit.
- 4.page 46 Modify 2nd FAN circuit
- 5.page 55 Modify CIR interface
- 6.page 54 Modify Audio Board interface
- 7.Delete R772/R774/R1096 and Q35 on page 48.
- 8.Backup express card and Wlan wake event signal leakage circuit and change net name "D_PCIE_WAKE#" on page 35 and 44.
- 9.Default for wake S3,backup for wake S4 circuit on page 36 and 61.
- 10.USB power change from +5valw to +5vsus on page 45.
- 11.Modify the resistors for CRT and TV disable on page 9.
- 12.Update CN29 for new symbol on page 45.
- 13.Modify EC pin out
- 14.Modify Mini PCIE power plan from SUS to RUN
- 15.Modify HDMI circuit
- 16.Change Y8 package to 5mm*7mm(H=1.2)
- 17.GPIO require from EC to SB Waiting S/W assign SB GPIO

(2005/09/23)

- 1.Change R162 from stuff to no stuff on page 13 .
- 2.Change R1354 pull-up power from +3VSUS to +3VRUN on page 44.
- 3. Pull " +1_5VRUN_DPLLA" and "+1_5VRUN_DPLLA" up to +1_5VRUN for high type and change CAP5/6 to CA on page 11.
- 4.Pull LVDS clock up to +1_5RUN and down to GND for high type base on design version 1.5 on page 8.
- 5.Add one inductance and one capacitor for SATSPLL power filter on page 36.
- 6.Add Function RUN_ON & AND_DOCK_S5_RST_100MS# & D_S5_PWRGD on page 44.
- 7.Detele HDCP_SCL & HDCP_SDA on page 44
- 8.Change MC_PWR_CTRL_MS# to MC_PWR_CTRL_MS; Change MC_PWR_CTRL_SD# to MC_PWR_CTRL_SD on page 56
- 9.Delete R925,R926 on page 56

(2005/09/27)

- 1.Delete R1739~1741 on page 9
- 2.Move three GPIO signals from EC to SB on page 35.
- 3.Change L4 and C142 value on page 11.
- 4.Add two 0ohm resistor for backup S4 wake event on page 61.
- 5.Modify Docking DVI chip from siil70B to siil162
- 6.Modify FAN circuit
- 7.Change CAP to FB on Audio internal speaker connector
- 8.Page 53 USB HUB 2.0->1.1

(2005/09/30)

- 1.PR407 change 0.012 ohm into 0.01 ohm
- 2.PQ3 change FDS6675A into SI4425BDY
- 3.PF1 change 8A into 10A
- 4.PD11 change MMVZ5231BPT into MMVZ5235BPT
- 5.PCN2 change package
- 6.De1 PQ75,Change PQ72,PQ74 to POWERPAK package
- 7.Add PC374,PC375
- 8.Modify GFX/HDMI circuit,review bypass and reciver RES.
- 9.Modify Docking pin out(Alex chen)

(2005/10/03)

- 1.Modify VRAM DDR3 Address pin swape(Alex chen)

(2005/10/04)

- 1.Schematic page swape
- 2.Modify Audio circuit
- 3.Modify VGA circuit
- 4.Modify SATA/PATA circuit
- 5.Modify SB SATA interface add SATA AC Coupling cap

(2005/10/06)

- 1.Modify Power circuit
- 2.Modify Audio circuit
- 3.Modify VGA circuit
- 4.Modify Mini PCIE Circuit
- 5.Delect R27,R130,R1772,R1773 and add the circuit for reboot.
- 6.Delect SM_VREF buffer circuit ,because the DDRDIMM_VREF can meet specification on page8.

(2005/10/07)

- 1.Modify CIR circuit ,change polyswitch
- 2.Modify GFX VRAM pin swape
- 3.Modify docking circuit
- 4.Add c? beside MDC Power on page 46
- 5.Detele R963 on page 47
- 6.Detele R1093,R1095,R1097; Detele C840,C834,C832,C1134 By on page 50
- 7.Change R1307 form 649 to 620 on page 51
- 8.Update DVI_TMDS* Net Name on page64

(2005/10/11)

- 1.Detele C836; ADD two 4.7K pull-up resistors to SMBUS on page 50
- 2.Change R110 from stuff to NC according to intel WW 41 document on page 8.
- 3.Modify VGA circuit
- 4.HDMI RP122,RP123,RP124,RP125 pin1-pin4 & pin2-pin3 pin swape.
- 5.Modify Power circuit

(2005/10/13)

- 1.Detele C836; ADD two 4.7K pull-up resistors to SMBUS on page 50
- 2.Change R110 from stuff to NC according to intel WW 41 document on page 8.
- 3.Modify VGA circuit
- 4.Modify Power circuit
- 5.Modify I/O Board connentor
- 6.Updata OrCAD symbol CN1,CN2,CN14,CN18,CN25,CPU,NB,Codec
- 7.Add Screw ,Boss,Power sequency page

(2005/10/19)

- 1.Change panel ID for Allen requirement on page39 .
- 2.Add 0.1u capacitance beside Vcppl&Vcpp2 on page 44
- 3.Change C954,C955 form 1u to 0.1u ; chang R931 form 10k to 43k on page 44
- 4.Add 2 capacitance of 0.1u beside +3VRUN on page 46
- 5.Change R1630 form 1.5k to 1k on 10/17 on page 46
- 6.change D62,D63 place on page 52
- 7.Add ten resistances on SD and MS signals according to MOR requirement.
- 8.Changed cap19/17 value from 150uF to 47uF according to MOR requirement on page52.
- 9.Add one 10uF capacitor and pull up SD_WP on page46.
- 10.Aadded R? 1R-000010X-F300 (1ohm 1%, 0603, 1/10W) according to latest checklist on page 40.
- 11.MIDIFY POWER CIRCUIT
- 12.MODIFY VGA circuit
- 13.MODIFY EC circuit
- 14.MODIFY SATA/ODD circuit

(2005/10/20)

- 1.Page43 PATA CD-ROM: CN32 Pin3(Audio_GND) connect to GND.
- 2.Page49 Mini-PCIE Card:only support S3 Wake On WLAN, so change Mini_PCiE_+3VAUX Default to +3VSUS (R1067 NC=>ON)(R1817 ON=>NC)

(2005/10/20)

- 1.Change the value of R91 to 1K and let PR126 no stuff.
- 2.Update connector pin connection according to Steve's comment.
- 3.Modify EC/Daughter Board connentor Circuit

(2005/10/24)

- 1.U126 pin27 Add 33pF and 12pF capacitor for RF frequency countermeasure.The small capacitance capacitor is put on close to 27 pin.
- 2.Delete L112.
- 3.A_GND GNDD connection through L(NC) at one point. Make this circuit on M/B. (This circuit is moved from Audio daughter board.)
- 4.U41 pin1 Change to following circuit.
- 5.U68 pin 1/pin 27 Add 1 kohm buffer resistance on IN_L. Add 1 kohm buffer resistance on IN_R.
- 6.Q112 It is necessary to check there is no chance not to be ON because of an internal resistance of Digital Tr(Q112) in the case of emitter follower.
- 7.U68 CP_GND do not have any connection to GND in schematics. There is no problem to connect A_GND.
- 8.Change the connection GNDD to A_GND.(C1291)
- 9.U50 Add the following RC filter(R:0 ohm,C:4.7uF) circuit between U50 4pin and MUTE_5
- 10.Modify VGA circuit

(2005/10/26)

- 1.Modify Power circuit
- 2.Delete TP682,TP684,TP619,TP621
- 3.Audio add E-CAP

(2005/10/27)

- 1.change PCI7412 to PCI8412
- 2.Connentor Pin swap CN21,for FFC pin1 to pin1,
- 3.Common chock pin swap L68, L120 for layout request
- 4.Modify Power circuit
- 5.Modify GFX circuit

(2005/11/01)

- 1.Modify GFX circuit (inluse ESD diode)
- 2.Modify Power circuit
- 3.Delete TP41,TP557
- 4.SATA CN63 Pin15.16.17.18.19.20 +3VRUN_SATA*->NC
- 5.SATA Delete Componment F9 & F10 & C791 & C792 & C1295 & C1296
- 6.Add SD LED
- 7.SPDIIF Add R1835 (MOR request) for matching the impedance

(2005/11/01)

- 1.Change C141 value from 0.1uF to 10uF on page 11.
- 2.Change R1307 value from 620_F to 649_F on page 51.
- 3.Add two resistors for clock amplitude tune on page 3.
- 4.Add one pull-low resistor in D_RUN_PWRGD on page64.
- 5.Modified for MOR requirement on page37 and page 39.
- 6.Delete LVDS_GPIO in EC pin85 and then make EC pin85 as Test Point.
- 7.Ducking Hot Dock issue add pull down 10K(R1889) on D_RUN_PWRGD

(2005/11/27)

- 1.MUTE_SW#(R1108) change from pull +ECVCC to pull +3VALW
- 2.CN42(FAN1)Pin swap
- 3.MOR COOLING UNIT,Add for 0V,1V,1.9V,5V control,solving 5V ringback
- 4.SD/MS LED(LED11) revise for too dark issue
- 5.BLUETOOTH LED(LED9) revise for too dark issue
- 6.SONY LOGO LED(U126)change from +3VRUN to +5VRUN,& change from AHC(CMOS) to AHCT(TTL)

(2005/12/08)

- 1.(U18)Change the connection for clock amplitude issue.(Add C1606,C1607,swape R1884,R1885 with L1,L2)
- 2.(U11)Update VDDR3 CLK terminal for G73(Add C1608,R1896,R1897)
- 3.(U12)Update VDDR3 CLK terminal for G73(Add C1609,R1898,R1899)
- 4.(VDDR3) RFMI(R1464),FBA_VBA2(R1463) change to NC
- 5.(EC)BATT_PRS# add circuit controlled by +3VALW(Add Q147,R1905)
- 6.(EC)PWRSW# (R700)pull up from +ECVCC to +3VALW
- 7.(EC)(Pull Down for EC strap issue)(Add RUN_ON2 R1903,IMVP_OK R1904)
- 8.(EC)Swap MUTE_SW# with IMVP_OK (pin8<->pin11)for EC strap(TEST_TP) issue
- 9.(EC)MUTE_SW# pull up(R1108) change from +ECVCC to +3VALW
- 10.(EC)Swap OVT_EC# with RUN_ON2(R713<->R714)for EC strap(DPLL_TP) issue
- 11.(EC)Change BIOS(U32->U34->CN14) net name SIO_FA[0..19] & SIO_FD[0..7]to XIO_FA[0..19] & XIO_FD[0..7]
- 12.(EC)XIO_FA4(R703) & XIO_FA5(R704)pull res change from 470K to 47K based on MS10 PVT revise
- 13.(EC) pin39 change from DOCK_RUN_RST to DOCK_RUN_RST#
- 14.(EC)PU CIR_ALPS_SW1 for EC strap(ISP_TP)(Add R1906)
- 15.(EC)pin156 ACIN Control by +3VALW(addQ148,R1907)
- 16.(GFX)FBCAL_PD_VDDQ add pull res (add R1900)
- 17.(GFX)reverse INV_EN_EC to conctect NONETNA2(add NC R1901)
- 18.(Audio)MUTE_5 add 10K RES to Q112(add R1902)
- 19.(GFX)PLT_RST# to GFX add a AND circuit(Add R1908,R1909,R1910,U127)
- 20.(HDMI)Del BUFRST# to microcontroller reverse gate(Del U124)
- 21.(Audio)modify capacitor value C1118 to 4.7u
- 22.(Thermal sanner)change part U8 (15-F75383M-0000->15-F75383M-1000)
- 23.(S-VIDEO ANALOG SWITCH)U77 change part U77 SN74CBT3257PW(NEW) <-> TS5A23157DGS(OLD)
- 24.(S-VIDEO ANALOG SWITCH)change throuth U77:PR_DDCCLK,PR_DDCDATA,MB_DDCCLK,MB_DDCDATA,GM_OR_NV_DDCCLK,GM_OR_NV_DDCDATA.
- 25.(SEMI-PNP)Modify SEMI-PNP circuit
- 26.(CRT)Modify CRT circuit:
- 27.(HDMI)U123 pin44 pull up res R1690 NC_10K_J <- NV72_10K_J
- 28.(HDMI)Modify Y8 circuit.
- 29.(PCMCIA)U62 pin12 connent to PLT_RST#
- 28.(Audio)Change part Q77,Q78,Q89,Q90,Q91,Q92,Q143,Q144(17-2SC5376-0000->17-PBSS251-5F00)
- 29.(SD)power control circuit R1630 (1K->330R)
- 30.(HDMI)U116 change part (SST89V54RD2-33-C-TQ <- NV_SST89V52RD2-33-C)
- 31.(Audio)Q112 change part (MMBT3906 <- 2SC5376)

(2005/12/15)

- 1.(POWER)Page 66----Change PR44 from 13K_J to 33K_J, Change PQ3 from SI4425BDY-T1-E3 to FDS6675A, Change PD1 from SSM344PT to SSM34PT.
- 2.(POWER)Page 67----Change PC350 from NC to 10U_25V_M_B, Change PR67 from NC to 0_J, Change PR63 from NC to 100K_J, change PR64 from 120K_F to 160K_F, change PR65 from 147K_F to 120K_F,Change from PJ29 to PR57 0_J, Delete PJ2&PJ4 and short, Delete PJ1&PJ3 and short, Delete PR414, Add PR422 1K_J.
- 3.(POWER)Page 68----Change PR79 from 56K_F to 47K_F, Delete PJ5&PJ6 and short, Delete PJ7&PJ8 and short.
- 4.(POWER)Page 69----Change PR305 from 8.2K_F to 6.2K_F, Delete PJ11 and short, Delete PJ9,PJ11&PJ37 and short.
- 5.(POWER)Page 70----Delete "Reserve for improve CLK_EN# wrong timing" circuit, Change PC276 & PC283 from NC to 10U_25V_M_B, Change PD18 & PD45 from SKS30-04AT-G to SSM34PT.Del PQ111,PR422
- 6.(POWER)Page 71----Change PQ104 from NC to 2N7002,Change PR404 from 62_J to NC, Change PQ50&PQ97 from IRF7807Z to IRF7402PBF, Delete PJ41 and short, Delete PJ28 and short,Delete PJ40 and short.
- 7.(POWER)Page 72----Change Power Limit circuit.(Add PR366,Del PQ109,PC188,PC189,PR207,PR208,PR212,PR213,PU14, change part:PQ110 NPN->N-MOS
- 8.(POWER)Page 73----Change PR227 from 56K_F to 47K_F, Change PR417 from 560_F to 2K_F, Change PR418 from 22K_F to 10K_F, Delete PJ32,PJ33&PJ35 and short, Delete PJ34 and short.
- 9.(CKG) Del C1606,C1607,R1884 and R1885 on page 3.
- 10.(CPU) Add 0.1uF capacitor(C1610) for GTLREF on page 5.
- 11.(Docking)Change Net From DK_BAY_PWEN to DK_BAY_PWREN
- 12.(Docking)Change Net From DK_BAY_ID# to DK_BAY_ID0#
- 13.(Docking)Change Net From AND_DOCK_S5_RST_100MS# to AND_DOCK_S5_RST_500MS#
- 14.(Docking)Change Net From DK_BAY_ID# to DK_BAY_ID0#
- 15.(GFX)Modify BOM configuration for G73M-U(BLOCK DIAGRAM).
- 16.(GFX)Modify PCI_DEVID[3:0]="1001"->9 for G73M-U.
- 17.(GFX)Add pull down 10K ohm resistor to DOCK_SEMI_PNP. (R1911)
- 18.(GFX)Update the pannel ID Spec.
- 19.(GFX)Change the reset signal to PCI_RST for U116 and U117(Nvidia suggestion).
- 20.(EC)Add DIP SW17(HDS401-E) for Instant ON selection.Delete R717,R716 change from CA_100K_J to 100K_J
- 21.(EC)Change CIR_ALPS_SW0 to SW_CIR00 for the same as IR module net name
- 22.(EC)Change CIR_ALPS_SW1 to SW_CIR01 for the same as IR module net name
- 23.(EC)Change CIR_ALPS_SW2 to SW_CIR02 for the same as IR module net name
- 24.(EC) Change CIR_ALPS_WAKE# to PWR_CIR# for the same as IR module net name
- 25.(EC)Change LIDIN# power source from +3VALW to +ECVCC due to SW/Kenny request
- 26.(EC)PWRSW# Pull High change from +3VALW to +ECVCC
- 27.(EC)Add KSO15 and redefine CN45 Pin4 ~ Pin6 for SW/Kenny Request
- 28.(CIR)Change EC to CIR connentor CN61 net name
- 29.(CIR)Add PWR_CIR# pull up RES R1913
- 30.(GFX)U8 modify
- 31.(EC)System ID pull up power source change from +ECVCC->+3VALW
- 32.(Audio)CVREF bypass CAP change from C863(10U)->(1U)
- 33.(Mini PCIE)WIRELESS Add R1912 pull up RES.
- 34.(EC) Add +ECVCC discharge RES (R1914)
- 35.(Touch Pad)LIDIN# pull up from +3VALW ->+ECVCC
- 36.(EC)Q147,Q148 change part from P-MOS->NPN
- 37.(SB) LVDSGPIO R1887 change to NC

(2005/12/21)

- 1.(EC)12/20,40 Revise SW17 from HDS401-E to HDS402-E_SW-SMD4 cause the vendor has stopped producing HDS401-E.
- 2.(EC)12/21,43 Revise C802/C803 from 10pf to 15pf due to Steve's SI test report.
- 3.(POWER)Page 67----Del PR422
- 4.(POWER)Page 69----Change PD19 to PD48
- 5.(POWER)Page 72----Change PU22A to PU15A, Change PU22B to PU15B
- 6.(POWER)Other-----Add 32mil test point for BFT test
- 7.(MDC)MDC connentor change to P/N: 1N-0012000-F0X0 ,BOSS1/BOSS2 P/N:1M-1A40M20-3100) the same with MS10
- 8.(CARD BUS)CARD BUS control change PCI7412 to 8412
- 9.(SB)RP95 pin swape for Layout request

(2005/12/30)

- 1.(GFX)Modify Si11162 power net SILL162_PVCC.
- 2.(GFX)Add FBA_CLK0_RC and FBA_CLK1_RC net name.
- 3.(GFX)Modify R378,R380,R1871,R1872 from 40ohm to 60ohm for Nvidia suggestion.
- 4.(GFX)Remove Si11162 and other parts to cancel G72M DVI Function.
- 5.(GFX)Add two Inverter gate to prevent the glitch from Silicon 1930.
- 6.(GFX)Update the reset signal of HDMI UCODEC,HDMI Microcontroller and HDMI Silicon 1930.
- 7.(GFX)Remove C432,R270,R274 on G73M SKU.
- 8.(GFX)Add TP682, TP678 test point because MIOBD7 and MIOBD10 unused.
- 9.(GFX)Modify HW strap for Infineon VRAM and update the BOM configuration in block diagram page.
- 10.(GFX)Change ESD diode D78,D79,D80 to meet the HDMI Spec.
- 11.(GFX)Delete the page 33(DVO-TMDS Si11162) for layout space.
- 12.(GFX)Add 1 switch to divide DVI DDC from HDMI DDC.
- 13.(GFX)12/27 Remove R195,R196,R1729,R1730 and C284 for G72M DVI funtion missing.
- 14.(GFX)Change R1592 from 360 ohm to 390 ohm for Silicon Image suggestion.
- 15.(GFX)Modify the INV_EN_EC to control INV_BRADJ for the Nvidia glitch issue on MS10.
- 16.(POWER)Page 71----Change PQ52,PQ112 from IRF7807Z to IRF7402PBF,Change PQ97 from IRF7402PBF to IRF7807Z.
- 17.(POWER)Page 72----Change PD52,PR420,PC374,PQ110 to NC.
- 18.(POWER)Page 67----Change PR49 from 160K to 187K, Change PR52 from 100K to 120K.
- 19.(ICH7)12/23 Change U30 and R1183 to NC and change R1184 to stuff on page 39.
- 20.(ICH7)12/23 Add two 2N7002 for leakage on page 38
- 21.(camera)Add 10uF capacitor for camera power,and add modify OCP circuit (add u133,del Q79,Q80)on page 50.
- 22.(CKG)12/23 change dumping resistor from 33 ohm to 100ohm and add FB between dumping resistor and clock generator for MOR requirement on page 3.
- 23.(CKG)12/28 Del 27MHZ circuit for Nvidia on page 3.
- 24.(USB)12/28 Change USB connectors to white type on page 52.
- 25.(EC)12/22,45 : Revise net name from FAN1_PWM to 2ND_FAN_PWM for error correction.
- 26.(EC)12/22,46 : Remove R1915 for moving pull high R from connector(CN68) side to EC side
- 27.(EC)12/22,47 : Add pull +ECVCC high R for moving from connector(CN68) side to EC side
- 28.(EC)12/23,48 : Revise H_RCIN# to EC_RCIN# and H_A20GATE to EC_A20GATE for matching leakage-proof circuit in P32
- 29.(EC)12/23,49 : Revise 2ND_FAN component to NC due to Ted request 12/22. (R1920-R1923,R1767,C1615,C1616,C1618,Q150,D87,CN65)
- 30.(EC)12/23,50 : Revise net name from FAN2_DAC to MOR_FAN_DAC due to Ted request 12/22.
- 31.(EC)12/23,51 : Revise net name from FAN2_DAC_OP to MOR_FAN_DAC_OP due to Ted request 12/22.
- 32.(EC)12/23,52 : Add 0 ohm(NC) for improving clock skew of PCLK_JIG.
- 32.(EC)12/23,53 : Revise R693,R1904,1903 from 10K to 100K for improving driving ability
- 33.(EC)12/23,54 : Add 1k ohm for avoiding EC directly short to GND.
- 34.(EC)12/26,55 : Change CN62 from HS8202E to HS8102E due to Mechanical 12/23 outline file
- 35.(EC)12/26,56 : Due to leakage of original circuit we revise 12/23 BATT_PRS# controlled by ALW power well circuit.
- 36.(EC)12/26,57 : Due to leakage of original circuit we revise 12/23 ACIN controlled by ALW power well circuit.
- 37.(EC)12/27,58 : D_S5_PWRGD add pull down 100k ohm due to Hibino san request(12/26 mail).
- 38.(EC)12/28,59 : Delete R1540 due to too dark issue
- 39.(EC)12/28,60 : Add PWRSW# test point due to BFT request.
- 40.(EC)12/28,61 : Change LED11 from HT-110UYG to HT-110UY due to error color correction.
- 41.(EC)12/28,64 : Change BT LED power source from +3VRUN to +5VRUN and R1839 from 68 ohm to 82 ohm due to too dark issue.
- 42.(EC)12/28,65 : Add ESD protector of SD LED due to Jacky Su/EMI request on 12/28.
- 43.(EC)12/28,66 : Add ESD protector of BlueTooth LED and WLAN LED due to Jacky Su/EMI request on 12/28.
- 45.(Ducking) Page64 CN30 pin 75,pin76 change net name NV_I2CB_SDA->DVI_I2CB_SDA NV_I2CB_SCL->DVI_I2CB_SCL
- 46.(GFX)Modify the INV_EN_EC to control INV_BRADJ for the Nvidia glitch issue on MS10.
- 47.(GFX)EMI suggestion:mount Cap.C1592,C1595,C1598,C1601.
- 48.(GFX)EMI suggestion:add cap.0.1uF on LCDVCC near CN3.Mount C1558 near CN49.
- 49.(GFX)EMI suggestion:add EMI bead on HDMI +5VSUS before C1452,and near CN60.reserve cap.0.1uF on +5VRUN near F1.
- 50.(GFX)EMI suggestion:add ESD Diode for AV_IN_GND.
- 51.(W-LAN)Page 49.Change R1912 from 1M to 100k ohm(Nishio San Request)
- 52.(W-LAN)Add FET on MINI_CARD_LED# between CN18 pin 44(P.49) and Q140 2pin(P.63) and control FET by using WLAN_EN that Wireless Off Control signal from EC .(Nishio San Request worry about only SW Driver control.)
- 53.(W-LAN)Prepare big Capacitor pad 22uF(1206) pad for MINI_PCIE +3.3V and MINI_PCIE +1.5V for each. Because .1ln is bigger than .1labg from point of view of power consumption.
- 54.(SD)change SD socket to 67913-0009(easy repaiy issue)
- 55.(LAN).XTAL Y6 Load CapC1034,C1035 change 22pF->27pF

(2005/12/31)

- 1.(POWER)Page 67----Change PR49 from 187K to 160K, Change PR52 from 120K to 102K.
- 2.(POWER)Page 72----Change PC368 from NC to 2.2U_10V_M_B
- 3.(EC)12/30,67 : Change R1920 from NC_1K to 1K due to error correction.
- 4.(EC)12/30,68 : Change TP785 net name from FAN2_DAC_OP to MOR_FAN_DAC_OP due to error correction.
- 5.(EC)12/30,69 : Swap CN68 for change T/P FFC from bending to no bending.
- 6.(EC)12/31,70 : Add constant current circuit MAX1916 due to MOR request.
- 7.(GFX)EMI suggestion:Add 33pF Cap to SVIN_Y_1 and SVIN_C_1.
- 8.(GFX)EMI suggestion:Change C1516,C1517,C1518,C1566,C1567,C1568 from 0.1uF to 220pF.
- 9.(GFX)EMI suggestion:add ESD Diode for SVIN_Y_GND and SVIN_C_GND.
- 10.(GFX).Add 1uF capacitor(NC) to VRAM_VREF for VRAM Max Load Drop.
- 11.(GFX).Add two resistor to LVDS CONN pin6 for Gamma control.
- 12.(Audio) Modify CN64 pin definf
- 13.(Audio)Change audio amp from MAXIN to TI
- 14.(USB)Delete EXT USB connentor (MB CN29),and move USB signal to CN64.

(2006/01/03)

- 1.(GFX)page 17.Add MIOB_CLKIN (R1939)10K ohm to GND
- 2.(GFX)page 35.Add NV_HDMI_DET_5 (R1940)100K ohm to GND
- 3.(EC)page 63.Add PWRSW# (TP846) Test Pad on BOT side
- 4.(ESD)page 63.Change Part D94,D95 from PACDN042Y3R to SM05.TCT
- 5.(ICH7) page 37 INT_PIRQE#_R conctect to GND(R1887) NC->0R
- 6.(GFX) page 25 (+1_8VRUN) CAP20 change 47uF to 150 uF

(2006/01/04)

- 1.(Oide)page 50.CN21.pin swape for ME request

(2006/01/20)

- 1.(Power)page 70.PR138 change from 13K to 16K due to 青建德 revise on 1/20.

(2006/01/21)

- 1.(ICH)page 37.Change R1886 from NC to 0 ohm due to control Gamma function.
- 2.(OIDE)page 50.Change F10 from 1206L150 to 1206L035 due to short current protect.

(2006/1/12)DVT-2

- 1.(GFX) For some HDMI device no support detect pin function issue, (1)Page 20 NV_GPIO6 del TP610,add off page port. (2)Page 35 Add backup circuit,NV_GPIO6(level shift) to switch(U136 pin1)Add part:Q156,Q155,R1942,(NC)R1941
- 2.(GFX)Page 35 HDMI 12C double pull up issue change R1611,R1612 NV->NC, because page 20,R1385,R1386 still pull up.
- 3.(Audio Conn)Page 59.For Audio Board USB2.0 HUB request, (1)CN64 pin 16 change GND to +3VSUS. (2)add FUSE(F9),and bypass CAP(C1641)
- 4.(CIR) Page 54 For BFM request,add CIR test pad (TP847-TP856)
- 5.(GFX) Page 34 Modify ESD diode (U128)depend on HDMI spec(C<50 pF) change part uClamp0504A->RClamp0514M (Modify Layout & BOM)
- 6.(SATA) Page 42 Modify SATA connentor pin define,pin swape and add power pin to meet 7200RPM HDD current(MAX 5.2A/2 HDD)
- 7.(SATA) Page 38 SATA signal Eye test Fail issue,change C724-C727,C1549-C1512 from P/N:1C-2B20392-K000(0402)->P/N:1C-2B30392-K001(0603) the same with MS10

(2006/1/16)DVT-2

- 1.(FAN-2) Page 62 Modify second FAN2 short with FAN1 issue
 - 2.(FAN-2) Page 62 FAN2 component cost down Q152,Q153,R1924,R1925 change to NC
 - 3.(SD LED) Page 63 LED11 change part HARVATEK_HT_110UY ->HARVATEK_HT_110Y
- (2006/1/18)DVT-2
- 1.(ICH7) Page37 For support LVDS_GPIO function,ICH7 INT_PIRQE#_R pull up RES.R1886 change 0R->NC
 - 2.(FAN-1) Page62 Modify fan speed feedback function,stuff C1521
 - 3.(W-LAN) Page49 For BFT test request,add wake on W-LAN test item,add Test Pad TP858
 - 4.(Audio) Page55 for Audio jack ESD issue,change Q117,Q118,Q119 form 17-2N70020-0000 ->17-2N7002K-0000
 - 5.(Oide) Page50 For I/O current protect request.Add F10, (This part only for placement,Wait to change part of I hold=0.35A,I trip=0.7A)

(2006/2/27)

- 1. Add doide for fan inverse current on page 62
- 2. Add capacitor 1uF for cooling unit on page 62.
- 3. Add capacitor 1000pF for fan noise on page 62 and should place colse to EC pin.
- 4. Chagne Oide power from +5VRUN to +5VSUS on page 50.
- 5. Audio coupling capacitor co-layout on page 56.
- 6. Backup 10uF capacitors for 22uF shortage on page 6.
- 7. Add discharge resistor for camera on page 50.
- 8. Change power plan for leakage issue of USB hub and change the fulse specification on page 54 , CN61 pin10 trace shold place same as pin1.
- 9. Add 6 fulse for FFC short issue on page 63.
- 10.Chagne CAP5 to "CA"
- 11.Add 2.2uf and 0.1uF capacitor for SMK power and add optional select for Alps pull-high power.

(2006/3/3)

- 1.(VIDEO)Modify the HW strap of VRAM for PVT
- 2.(VIDEO)Modify R1463,R1464,R1475,R1480,R1482,R1493 for 16Mx32 and 8Mx32 VRAM configuration
- 3.(VIDEO)U136 change switch control from NV_HDMI_DET_5 to NV_GPIO6
- 4.(VIDEO)Add two 0 ohm resistors to avoid the switch for NV_I2CB because G72M only support HDMI
- 5.Change codec CIS symbol to four plus.
- 6. Add open jump on RTCRST# net on page 38.
- 7. Delet fan2 circuit and change the pull-high resistor of fan_tach from 10K to 4.7K.
- 8. Back up logo led circuit for GMT solution on page 63.
- 9. MS_R and SD_R net name changed each other on page46.
- 10.Change connector S/N from 1N-0010000-M0X0 to 1N-0010000-MWG0 for S/N wrong on page32.
- 11.Change CN68 S/N from 1N-0010000-M0X0 to 1N-0010000-MWG0 for S/N wrong on page63.
- 12.Change the resistor (R1839) of bluetooth to 200ohm for too light issue on page 63.
- 13.Change the resistor (R1879) of SD card to 33 ohm for too dark issue on page 63.

(2006/3/9)

- 1. Change C1521 from Y5V to X7R on page 62
- 2. R585 change from 20K_J to 22K_F
- 3. Boss4 and Boss5 change to "NV73_" on page 74.
- 4. Add one test point on signal "2ND_FAN_TACH" on page 60.
- 5. Add 4 test points on CN21 connector for TE test on page50.
- 6. Change net name from "EN_EXT_DEV_SENSE#" to "EN_EXT_DEV_SENSE" on page 30,60 and 64.
- 7. Delet R1906 on page 60 for CIR double pull-high issue.
- 8. Change R1913 from 10K to 100K on page 54.
- 9. Change CN19 parts for SMT issue on page50.
- 10.Change CN64 PIN16 from +3VSUS to GND and change PIN6 from USB_PP2 to USB_VCC2, Shift Pin 6&8 to Pin 8&10, Delet F9 and C1641 on page59.
- 11.Backup fusle for HDD voltage drop issue on page42.
- 12.Update U117 CIS symbol on page 34.
- 13.Update CN60 CIS symbol for SMT issue on page34
- 14.Add two 0ohm resistors for Viao loge soft start issue on page 63 and page60.
- 15.(Power)Page 69-----Change PR91 from 15.8K_F to 16.5K_F.
- 16.(Power)Page 70-----Change PR299/PR114/PR115 to 10 ohm, Change PR300 to 0 ohm, Change PC127 from NC to 1000P_50V_K_B, Change PC126 to PR397 10K ohm. Change PR387 to 2.7K ohm.
- 17.(Power)Page72----Change PC326&PC327 from 0.1U_16V_Y_Y to 0.1U_16V_M (X5R)
- 18.(Power)Page71----Change PQ97 from IRF7807Z to IRF8113.
- 19.(Video)Page 20,R1820change to NC,because The MS20 CEC line capacitance = 777pF is much bigger than 100PF spec. After remove this resistor, CEC cap reduced to 39PF. Pass.(This GPIO11 is no function on our system, Silicon Image suggest remove it.)
- 20.(Video)Page 74-BOSS4,BOSS5 change part name from NV73_->TV_
- 21.(Video)Page 32 change part name from NV73_->TV_
- 22.(Video)Page 32 CN67,change PCB Footprint to co-layput "molex" & "Foxconn"part
- 23.page 63 CN68 change PCB Footprint to co-layput "molex" & "Foxconn"part
- 24.page 15 add C1661 (0.1uF) close CN2 pin1 (DDR2_VREF) for voltage level noise debug.

(2006/3/11)

- 1.Page 62 C1658 change to NC
- 2.Page 56 CAP24,CAP25 change to NC
- 3.Page 70 PR397 change part 10K(5%) to 10K(1%)
- 4.(VIDEO)Page 35 R1940 change part name NV_100K_J to NV73_100K_J
- 5.(VIDEO) page 27,Page 28 PVT EMI recommend(NC_ ->NV_):C1590,C1591,C1593,C1594,C1596,C1597,C1599,C1600

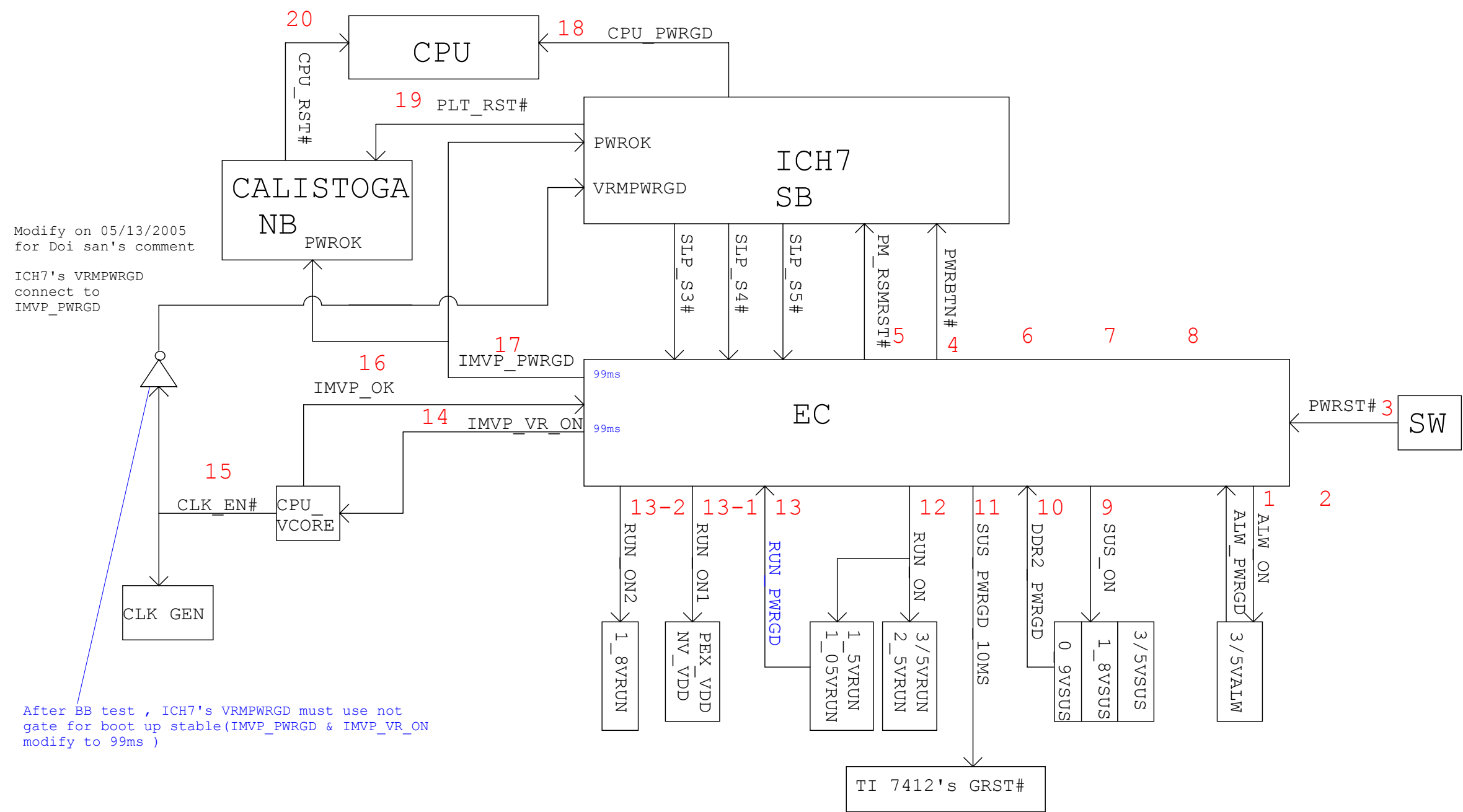
(2006/3/13)

"Not neet to modiy BOM and Layout "

- 1.change title block ver "1.0" to "0.40"
- 2.page 34.HDMI circuit, change net name(1)HDMI_+5VSUS->HDMI_+5VRUN (2)HDMI_+5VSUS1->HDMI_+5VRUN1

1.(page60)FAN noise issue:Add 1000pF(C1662)closc EC Add 1000pF(C1666)closc PVT rework location(backup only) on net FAN1_TACH(fan feedback),and remove C1657 on net FAN1_PWM(EC to FAN control) *PVT already modify(Rework Notice item#2)	17.(page63)Power Button Board Connector back up power plan bypass cap C1507 change to NC (modify BOM change part name NC_)
2.(page 70)TV turner noise issue: (1)Add PR424(2.2 ohm), PC378(47pF) on net MAX8771_LX1, (2)Add PR425(2.2 ohm), PC379(47pF) on net MAX8771_LX2 (3)PR299 change value from 10 ohm to 0 ohm *PVT already modify(special noties V0.8)	18.Y7 (6MHZ_20P_30PPM)change part number from secondsource to main source(buyer request) P/N:(1F-X00006M-3001(AKER) ->1F-X00006M-3002(TXE) Footprint:(xtal_4p_244_284x205 -> xtal_4p_232_276x197) *The second already verify on DVT & PVT
3.(page54)WA of InstantOn later(1) IR receiver connentor side add N-MOS 2N7002(Q157) for 3V->5V level shift *PVT already modify(Rework Notice item#3)	19.(page43)ESD 10KV on ODD reboot issue (1)add C1668(100pF) on net ODD_RESET# (2)add C1667(0.1uF) on net +5V_RUN
4.(page60)WA of InstantOn later(2) EC (U32)GPIO18(pin85)contact to 2N7002 pin1 *PVT already modify(Rework Notice item#3)	20.(page73)NV_VDD on G73M-U power noise issue, change PR417 (PU16-FB2) from 2K to 2.1K (to setting NV_VDD voltage on G73M-U from 1.2V to 1.21V)
5.(page29)Modify BOM to desable HDMI connentor SEMI PNP Hot plug detect function:(backup) (1)U108 change part name to NC_ (not stuff) (2)Add R1952 (0 ohm) link U84 pin4 to U73 pin2	21.(page26)NV_VDD on G73M-U power noise issue,modify BOM configuration, (1)G73M-U (H) C352,C362,C363,C364 on 22uF / X5R / 0805(1C-2B70226-M100) (2)G72 (L) / G73 (M) C352,C362,C363,C364 on 10uF / X5R / 0805(1C-2B70106-M100)
6.(page32)TV module modify BOM roul (1)Mini PCI socket circuit group change part neam from TV_ to normal. (2)Special mini stereo jack and S-VIDEO in group change part name from TV_ to JDTVNC_ (JP digital tuner sku NOT stuff)	22.(page31) CN3 (LVDS CONNECTOR) update OrCAN symbol
7.(page32)TV Tuner EMC request (1) add R1950(0 ohm) link net AV_IN_GND to GND (2) add C1663(470pF) link net AUDIO_IN_L_1 to AV_IN_GND (3) add C1664(470pF) link net AUDIO_IN_R_1 to AV_IN_GND (4) add C1665(100pF) link net VIDEO_COMP_1 to AV_IN_GND	
8.(page66)PD10 Change from 16-MM3216V-T100(Vz=15.3V~17.1V) to 16-MMP2524-6B00(Vz=16.8V) *PVT already modify(special noties V0.5)	
9.(page35)Desable HDMI connentor SEMI PNP Hot plug detect function(MOR request) change part name: (1)NV73 ->NV_:U136,Q155,Q156,R1940,R1941,C1616 (2)NV72 ->NC:R1946,R1947 *PVT already modify(special noties V0.4)	
10.R1493 change part name (G73Only_ ->NV73Only_) to meet BOM configuration *PVT already modify(special noties V0.6)	
11.(page57)Q86 change part from 17-MMBT390-6000 (MMBT3906) to 17-MMBT390-6K00 (MMBT3906K) *PVT already modify(special noties V0.1)	
12.Modify Bluetooth LED brightness (1)LED9 change part from 16-HT110NB-0000(Vendor P/N : HT_110NB) to 16-HT110NB-5000.(Vendor P/N : HT-110NB5) (The same with MS10) (2)R1839 change part from 1R-0000201-J200 (200ohm,5%,0402) to 1R-0000391-J300.(390 ohm,5%,0603) (The same with MS10)	
13.Modify SD LED brightness LED11 change part from 16-HT110Y0-0000(Vendor P/N : HT_110Y)to 16-HT110UY-0000.(Vendor P/N : HT-110UY)	
14.(page7~page13) updata U4(NB) part to meet KCL change from 12-0K58000-A300(945 PM ,QK5800,Version A3) to 12-0G82945-A301(945 PM ,QG82945PM (SL8Z4),Version A3)	
15.(page37~page41) updata U29(SB) part to meet KCL change from 12-0K17000-B000(82801GHM1,QK1700,Version B0) to 12-NH82801-0000(NH82801GHM,(SL8YR),Version B0)	
16.FAN Noise on Int.MIC (1)Cut-off frequency => 159Hz R1319 : 2.2k -> 1k C1232 : 2.2u -> 1u (2)Cut-off frequency =>7.2kHz R1318: 22k -> 10k C1230: 220p -> 2200p *MOR Nishio-san suggest 3/31	

MS20 Power On Sequerce Block Diagram



MS20 Power On Sequerce Timing

Version : 0.1
Modified date : 2006/4/6

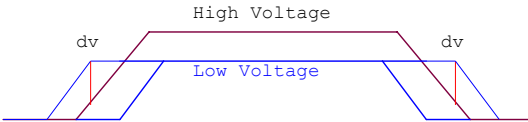
NOTE : (EC KB3910 Min. response time is 1ms)

- T00 : R=47K , C = 0.1uF is ENE recommand value please refer to KB3910B0-AN4A-200
- T01 : When RTC battery already is present, this timing is always meet specification, so we don't control it.
- T02 : ALW_PWRGD:H to PM_RSMRST#:H at least 5ms (Please refer to 16971 Page_300 of t205 timing) Doi-San request 10ms 05/17
- T04 : For MS01 SPEC Min. is 50 ms (Normal SPEC is 20ms)
- T05 : RSMRST# active High to SLP_S5# active High Max. is 110ms (Please reference Intel 16971 Page 301 of t232 timing)
- T06 (Please reference Intel 16971 Page 301 of t234 timing)
- T07 : For MS01 current SPEC Min. is 25 ms (Please refer Intel 16971 Page 301 t208 SPEC is Min 10ms)
- T08 : For MS01 current SPEC Min. is 1 ms (1ms is EC KB3910 at least response time)
- T09 : For MS01 current SPEC
- T10 : Please refer to Intel 16971 Page 300 of t214 timing
- T11 : Please refer to Intel 16971 Page 303 of t216 timing
- T12 : PM_RSMRST# ACTIVE HIGH TO PM_PWRBTN# ACTIVE LOW is 400ms (Normal SPEC is 110ms; Please reference Intel 16971 Page 301 of t232 timing)
- T13 : For MS01 current SPEC Min. is 700 ms (Normal SPEC is 1ms that EC can response)
- T14 : For MS01 current SPEC Min. is 5 ms
- DDR2 1.8V from 0V to 2V Max. is 2 ms please refer to Intel 16981 Page 304
- IMVP_OK is same with SB_PWRGD (reserved And Gate with SYS_PWRGD)
- In NV4X power sequence : NV_VDD , VRAMVDD, PEX_VDD and VRAM_TERM can ramping up anytime after +3VRUN starts ramping up. (Please refer to DG-00969_v05c Page 50 for NV4x GPU power sequencing description)
- T15 : Please refer to MAX8736 datasheet page 7 & page 25 Figure 8
- T16: Please refer to MAX8736 datasheet page 25 Figure 8
- T17 : Please refer to Intel CK410(14690) page 53
- T18 : The ICH7 drives PLTRST# active a minimum of 1ms when initiated through the Reset Control register I/O Register CF9h)
- CPUPWRGD is an output signal that presents a logical AND of the ICH7's PWROK and VRMPWRGD signals
- T20 : From ECRST# L->H to IMVP_PWRGD L->H. If EC's 32KHz is not stable, LPC I/F will hang. So the 1sec must be guaranteed. (Requested by Doi's san 05/13)

Remark: (Item1,2,3 add Diode; Item4,5,6 add dischage circuit; Item7 for implement TV)
SPEC please refer to Intel 16981 15.4 GMCH/ICH7M Platform Power -up Requirements)

- V5REF(+5VRUN) -> +3VRUN, dt:0.7mV
- V5REF_SUS(+5VALW) -> +3VALW, dt:0.7mV
- +2.5VRUN -> GMCH_VCC(1.05V), dt:0.7mV
- +1_5VRUN -> +GMCH(1.05V), dt:0.7mV
- +3.3VRUN -> +2_5VRUN, dt:0.3mV
- +3.3VRUN -> +5VRUN (VccLAN), dt:0.3mV
- +3_3VRUN -> +1_5VRUN (TV), dt:0.7mV

R/C delay
(47K/
0.1uF)



T00 within 10ns~2ms	T01 Don't control	T02 Min. 10 ms	T03 Min. 40ms	T04 Min. 50ms	T05 Max. 110ms	T06 1 - 2 RTCCCLK	T07 Min. 25 ms	T08 1ms	T09 Min. 10ms	T10 Min. 99ms
T11 Max. 50ns	T12 Min. 400ms	T13 Min 700ms	T14 Min 5ms	T15 typ 60us	T16 Min : 3ms Max : 8ms	T17 Max 1.8ms	T18 Min 1ms	T19 Min : 99ms	T20 Min :1s	